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Advanced electronic packaging materials: constitutive model, simulation, design and reliability

Edited by
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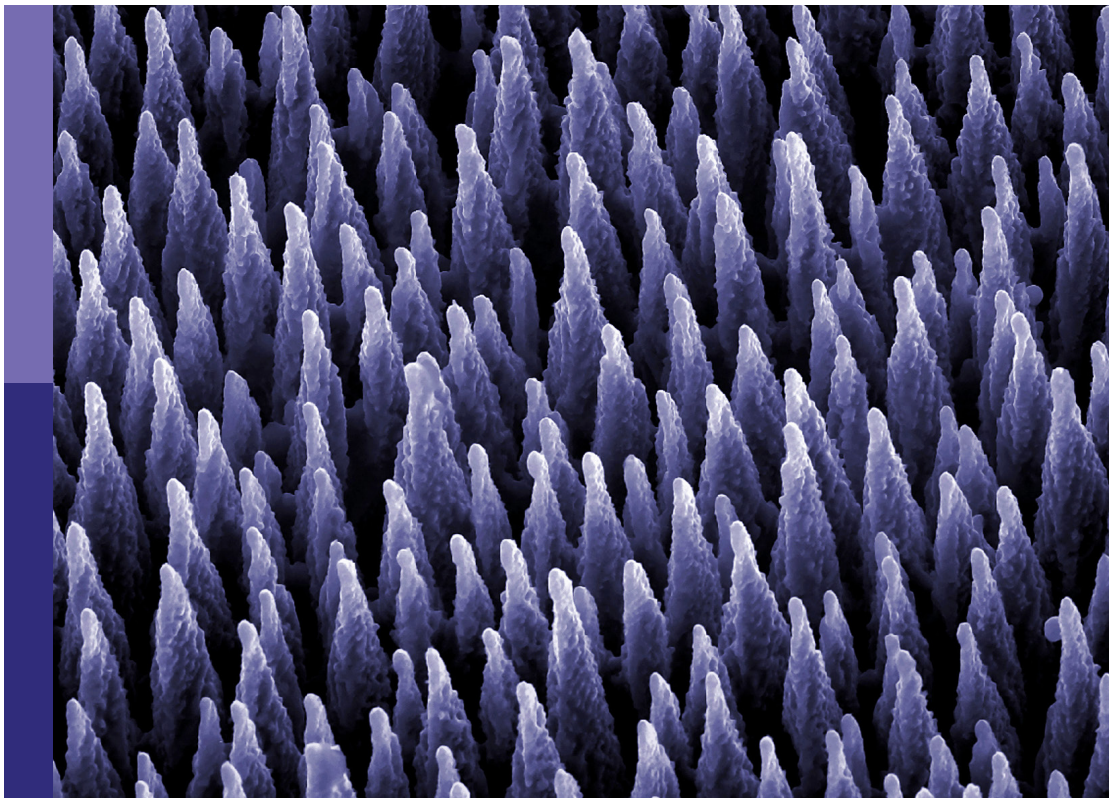
Published in
Frontiers in Materials



ISSN 1664-8714
ISBN 978-2-8325-7078-4
DOI 10.3389/978-2-8325-7078-4

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Advanced electronic packaging materials: constitutive model, simulation, design and reliability

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Citation

Su, Y., Long, X., Chen, C., Chao, X., Wan, B., eds. (2025). *Advanced electronic packaging materials: constitutive model, simulation, design and reliability*. Lausanne: Frontiers Media SA. doi: 10.3389/978-2-8325-7078-4

Table of contents

frontiers | Frontiers in Materials

TYPE Editorial
PUBLISHED 17 October 2025
DOI 10.3389/fmats.2025.1702323

OPEN ACCESS

EDITED AND REVIEWED BY
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RECEIVED 09 September 2025
ACCEPTED 07 October 2025
PUBLISHED 17 October 2025

CITATION
Su Y (2025) Editorial: Advanced electronic packaging materials: Constitutive model, simulation, design and reliability.
Front. Mater. 12:1702323.
doi: 10.3389/fmats.2025.1702323

Editorial: Advanced electronic packaging materials: Constitutive model, simulation, design and reliability

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KEYWORDS

advanced electronic packaging, constitutive modeling, multiscale simulation, reliability evaluation, diamond/copper composites

Editorial on the Research Topic
Advanced electronic packaging materials: constitutive model, simulation, design and reliability

Introduction

The relentless drive toward miniaturization, functional integration, and high-power density in electronics has placed unprecedented demands on packaging technologies. Beyond their traditional roles of electrical interconnection and protection, packaging materials must now ensure mechanical reliability and efficient thermal management under increasingly harsh conditions. This Research Topic, Advanced Electronic Packaging Materials: Constitutive Model, Simulation, Design and Reliability, gathers contributions that address these challenges from the perspectives of material innovation, constitutive modeling, numerical simulation, and service reliability. Collectively, they advance a holistic understanding of how microstructure, mechanics, and environment converge to determine long-term performance.

Multiscale constitutive modeling and simulation

Zhou et al. presented a comprehensive review of multiscale mechanics and numerical approaches for interconnect materials, integrating atomic-scale molecular dynamics, meso-scale crystal plasticity and phase-field models, and macroscopic constitutive laws such as Anand and unified creep plasticity. Their work emphasizes that predictive reliability requires explicit links between microstructural morphology, pore evolution, and macroscopic fatigue behavior, forming a coherent framework for simulation-driven design (Zhou et al.).

Complementing this, Zhou et al. proposed a fatigue lifetime prediction method for copper pillar bumps in 2.5D packaging. By employing extended finite element simulations of crack propagation, they showed how intermetallic compound (IMC) thickness governs

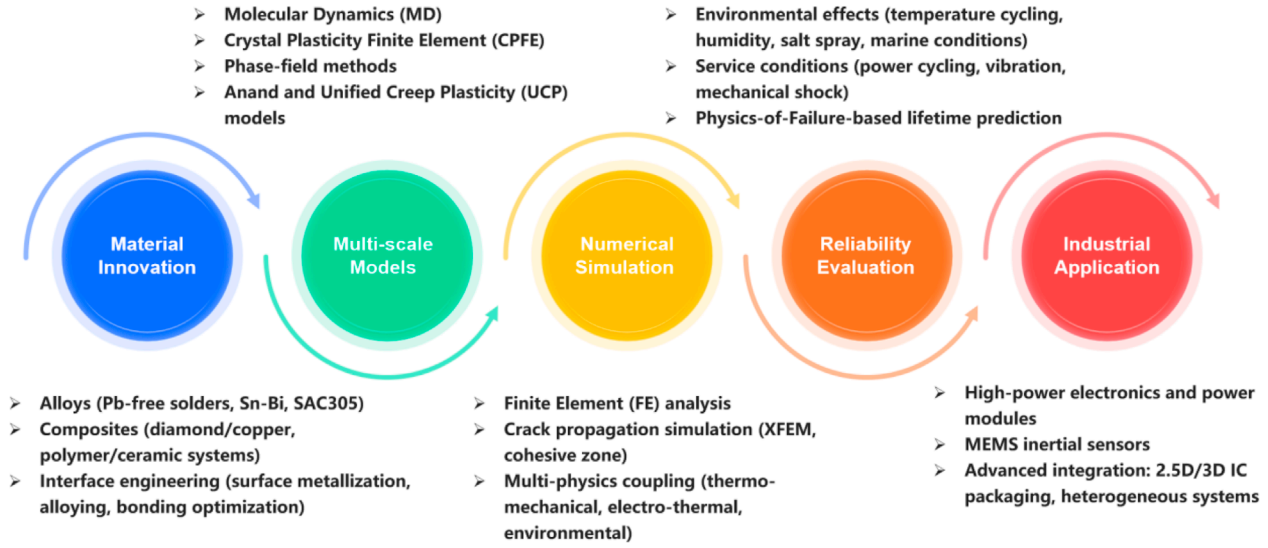

FIGURE 1
Flowchart with four interconnected stages: Material Innovation, Multi-scale Models, Numerical Simulation, and Reliability Evaluation, leading to Industrial Application. Each stage includes specific techniques and materials, like alloys, composites, finite element analysis, environmental effects, and various industrial applications.

fatigue performance. This work highlights the need to replace traditional solder joint life models with more accurate crack-propagation-based methods for advanced packaging (Zhou et al.).

Material innovation for enhanced reliability

Material development remains central to improving packaging performance. Yao et al. studied Sn-58Bi solders reinforced with Zn particles, demonstrating that 0.5 wt% Zn addition refines microstructure, suppresses IMC growth, and optimizes shear strength during long-term aging, whereas excess Zn leads to interfacial fracture. This illustrates how precise alloy design can balance ductility, interfacial stability, and reliability (Yao et al.).

Thermal management was addressed by Xue et al., who reviewed high thermal conductivity diamond/copper composites. By analyzing surface metallization, alloying strategies, and advanced sintering processes, they showed how interfacial engineering minimizes thermal boundary resistance and enables reliable integration into power electronic systems. Such work underscores the direct link between interfacial optimization and system-level thermal reliability (Xue et al.).

Environmental and service-dependent reliability

Reliability must also be understood in service contexts. Lang et al. reviewed degradation of packaging materials in marine environments, identifying chloride-induced corrosion, moisture-driven delamination, thermal cycling fatigue, and mechanical shock as critical mechanisms. They argue for multiphysics coupling models to predict long-term behavior under combined marine stressors (Lang et al.).

Liu et al. analyzed packaging structures of MEMS inertial sensors across consumer, industrial, and tactical applications. They showed how packaging-induced stresses and thermo-electrical coupling directly affect bias stability, noise density, and drift performance. Their findings reinforce that packaging is not passive protection but a determinant of sensor precision (Liu et al.).

Broadening reliability perspectives

This Research Topic also extends beyond conventional packaging. Mei et al. proposed an integrated methodology for bare die selection, combining risk analysis, microstructural evaluation, and reliability assessment. Their approach enables cost reduction while ensuring functional integrity in high-reliability systems (Liang et al.).

Meanwhile, Jia et al. studied hydrogen-induced cracking in pipeline steels, employing user-defined subroutines to model heterogeneous microstructures and crack growth. Although outside traditional electronics, their work illustrates how advanced constitutive modeling from packaging research informs broader structural reliability challenges (Jia et al.).

At the system level, Praful and Bailey reviewed wafer-level packaging warpage, a persistent challenge in fan-out integration. They highlighted modeling strategies—including emerging AI/ML methods—that provide new avenues for prediction and mitigation (Praful and Bailey). This review situates packaging reliability at the center of heterogeneous integration for high-performance computing and artificial intelligence.

To better illustrate the progressive relationship among material design, constitutive modeling, numerical simulation, reliability assessment, and applications, the overall framework of this Research Topic is summarized in Figure 1.

Concluding remarks

Together, the contributions in this Research Topic underscore three converging directions for advanced electronic packaging research:

- Multiscale integration–Constitutive models must explicitly couple microstructural evolution with macroscopic reliability.
- Material innovation–Alloying, composites, and interfacial engineering are indispensable for balancing performance and reliability.
- Contextual reliability–Environmental extremes and device-specific performance metrics must be embedded into design rules.

By spanning constitutive models, novel materials, environmental degradation, and system-level challenges, this Research Topic provides both theoretical insights and practical guidance. As electronics move toward heterogeneous integration and operation in extreme environments, the frameworks and findings presented here offer essential pathways for designing packaging materials and structures that are not only high-performing but also durable and sustainable.

Author contributions

YS: Writing – original draft, Writing – review and editing.

Funding

The author(s) declare that financial support was received for the research and/or publication of this article. This work was supported by the National Natural Science Foundation of China (52505158), the Qin Chuang Yuan high-level innovation and entrepreneurship talent project (No. QCYRCXM-2022-306), and the Natural Science Foundation of Chongqing (No. CSTB2022NSCQ-MSX0574).

Conflict of interest

Author YS was employed by Xi'an XICE Testing Technology Co., Ltd.

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Publisher's note

frontiers | Frontiers in Materials

TYPE Original Research
PUBLISHED 02 September 2024
DOI 10.3389/fmats.2024.1470365

OPEN ACCESS

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RECEIVED 25 July 2024
ACCEPTED 21 August 2024
PUBLISHED 02 September 2024

CITATION
Zhou Y, Liu Q, Ma T, Li S and Zhang X (2024) Lifetime prediction of copper pillar bumps based on fatigue crack propagation.
Front. Mater. 11:1470365.
doi: 10.3389/fmats.2024.1470365

Lifetime prediction of copper pillar bumps based on fatigue crack propagation

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2.5D package realizes the interconnection of multiple dies through Si interposers, which can greatly improve the data transmission rate between dies. However, its multi-layer structure and high package density also place higher reliability requirements on the interconnection structure. As a key structure for interconnection, copper pillar bump (CPB) has small size, high heat generation, and thermal mismatch with silicon chips. The thermal fatigue failure of CPB has gradually become the main failure mode in 2.5D package. Due to the small size of CPB and the large proportion of intermetallic compound (IMC) layers, the lifetime prediction method of spherical solder joints is no longer suitable for CPB. Therefore, it is necessary to establish a fatigue lifetime prediction method for CPB. This paper establishes a method for obtaining the lifetime of CPB based on the basic theory of fatigue crack propagation. Using the extended finite element simulation method, the crack propagation lifetime of CPB under thermal cycling was obtained, and the influence of different IMC layer thickness on the fatigue lifetime of CPB was analyzed. The results indicated that the fatigue lifetime of cracks propagating in the IMC layer is lower than that of cracks propagating in the solder layer, and an increase in the thickness of the IMC layer leads to a significant decrease in the fatigue lifetime of CPB. The lifetime prediction method for CPB proposed in this paper can be used for reliability evaluation of 2.5D package, and has certain reference value for the study of the lifetime of CPB.

KEYWORDS

2.5D package, copper pillar bump (CPB), IMC layer, extended finite element simulation, lifetime prediction

1 Introduction

With the increasing demand for product miniaturization, high I/O density, and heterogeneous integration, higher requirements have been put forward for the front end and back end processes of semiconductors. But currently, the process of transistors is approaching the physical limit, and the benefits of relying on reducing semiconductor gate width to increase integration are decreasing (Wong, 2021; Watanabe, 2009). Therefore, more and more manufacturers are shifting the direction of improving

integration and reducing chip size from front end processes to back end processes, hoping to break through the physical size limitations of chips with more advanced packaging forms. Among them, the 2.5D package can package multiple chips with different functions and structures onto a Si interposers, achieving heterogeneous integration (Lancaster and Keswani, 2018; Zhang et al., 2021; Dale et al., 2020). Due to the shorter distance between chips, this package structure occupies less space, and it has lower power consumption and better electrical performance compared to traditional package (Liu et al., 2016).

In order to realize the vertical electrical connection of 2.5D package, various bump interconnection technologies are used, mainly including copper pillar bumps (CPBs) and C4 bumps (Liu et al., 2016; Zhang et al., 2015). Among these bump technologies, CPBs are the interconnect bumps with the smallest geometric size, shortest pitch, and highest density. Compared with traditional spherical bumps, cylindrical CPBs have higher aspect ratio and can solve the ultra-fine pitch problem of high-density package. At the same time, the CPBs also have excellent electrical and thermal conductivity properties, and the lead-free solder cap can also meet the ROHS requirements. Therefore, CPB technology is more and more widely used in various types of 2.5D and 3D package, and has gradually become a key link in the package.

However, as the size of CPB continues to decrease, the operating current continues to increase, and the working environment temperature is also getting higher, which leads to some problems in the application of 2.5D package. Due to the harmful effects of Pb-containing solders on the environment and human health, Pb-free materials such as SAC305 have been widely used as substitutes for interconnect materials under the National Electronics Manufacturing Initiative (Long et al., 2023). The solder cap material for CPB generally uses lead-free solder materials such as Sn-Ag or Sn-Ag-Cu. The solder joint is prone to producing rich intermetallic compounds (IMC) during use. Under long-term high-temperature action, the solder cap may even completely transform into an IMC layer (Rao et al., 2016; Na et al., 2022; Koo et al., 2007). With the emergence of the IMC layer, the mechanical strength and fracture toughness of the solder joints will decrease, causing crack in the welding helmet to expand more easily and reducing its fatigue lifetime (Gong et al., 2024). In addition, the 2.5D package has a high density and a large heat generation of the chip. The difference in thermal expansion coefficient between the copper pillar in CPB and the silicon material is significant, resulting in a serious thermal mismatch problem in this structure. As its size decreases, the failure of the CPB has become one of the main failure modes of 2.5D package (Jing et al., 2014). Therefore, studying the fatigue failure of CPB plays an important role in improving the reliability of 2.5D package.

Some authors have already noticed that the presence of IMC layers can affect the mechanical properties and reliability of CPB. Kwon et al. (2016) found that under thermal cycling conditions, an IMC layer is formed at the interface between solder and copper, and the thickness of the IMC layer also increases with time and temperature. When the z-direction stress caused by thermal expansion acts on the interface, the crack would propagate along the depletion zone, and eventually microcrack failure would occur. Ajay Kumar and Dutta (2018) analyzed the growth kinetics and shear deformation tests of IMC in thin Sn-3Ag-0.5Cu joints, and inferred that the increase in IMC content caused by heat treatment would lead to a deterioration of the mechanical properties of the joint due to the presence of initial microcracks. Zhu et al. (2020) conducted shear fatigue tests on CPB with different thicknesses of IMC layers and found that their fracture toughness decreased with increasing IMC thickness. They also applied the Coffin-Manon model to predict the fatigue lifetime of CPB, but the accuracy was slightly poor. Li et al. (2020) found that there are two locations for crack propagation at CPB, namely, Sn-Ag solder joint and IMC bump. They also compared the lifetime prediction results of the Darveaux model and Schubert model, and found that the latter should be more suitable for CPB, but both have significant deviations.

At present, many research has been conducted on traditional spherical solder joints. Based on different theoretical systems, lifetime prediction models suitable for different types of solder joints have been proposed. But among these models, most only consider the constitutive model of solder (Su et al., 2019). Generally speaking, in current 2.5D package, the diameter of the more commonly used CPB is about 30 μm, the diameter of the C4 solder ball is about 100 μm, and the diameter of the BGA solder ball is several hundred microns. The volume of C4 solder joints and BGA solder joints is hundreds or thousands of times that of CPB. The proportion of the IMC layer in CPB is much larger than that in BGA solder joints (Yu et al., 2024; Chen et al., 2022). The impact of the IMC layer on the thermal fatigue of CPB cannot be ignored. If the previous lifetime prediction model is completely applied, it may lead to significant prediction deviations. Therefore, it is necessary to develop a new life prediction method for CPB.

In this paper, the CPB within the 2.5D package is focused upon. An equivalent model was utilized to simplify the complex model, and thermodynamic simulation calculations were carried out. The accuracy of the simulation model was verified by measuring the warpage of the chip through moire interferometry. The extended finite element method was employed for fatigue simulation to derive the fatigue lifetime of the CPB. And an analysis of the impact of IMC layer thickness on the fatigue lifetime was also conducted. The proposed fatigue lifetime prediction method for CPB serves as a reference for the reliability assessment of 2.5D package designs.

2 2.5D package equivalent model simulation

2.1 Obtaining equivalent model parameters

The research object selected in this article is the high-density package vega 56 graphics card core produced by AMD. The number of through-silicon vias (TSVs), C4 solder joints, and CPBs in this device is very large, and the sizes of these structures are in the tens of microns. Compared to the entire package, they are all small structures. The method of establishing equivalent models can be used to simplify complex models into simple structures. The following structures need to be simplified: the interposers where the TSVs is located, the C4 solder joints with underfill, and the CPBs with underfill.

Taking the Si interposers as an example and referring to the equivalent parameter calculation methods in Chien et al. (2011)

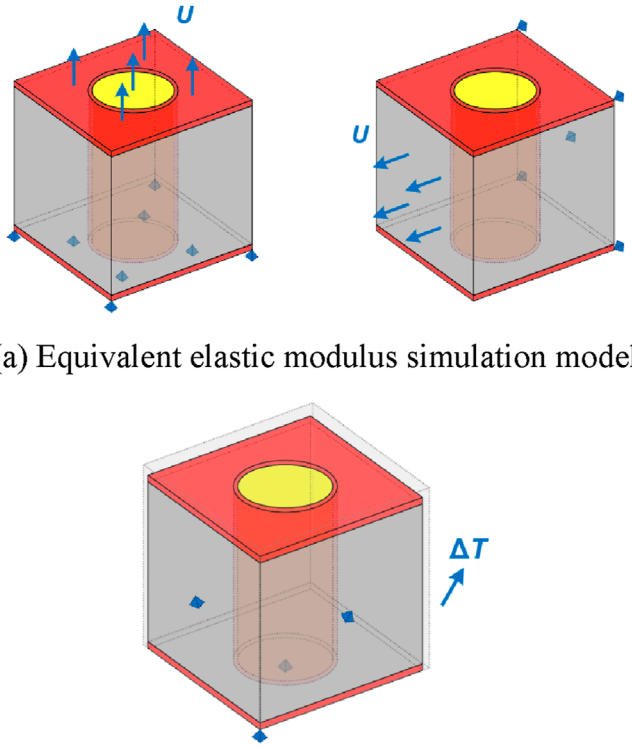


FIGURE 1
Equivalent simulation model. **(A)** Equivalent elastic modulus simulation model. **(B)** Equivalent thermal expansion coefficient simulation model.

and Chen and Wu (2015), the calculation formula of its equivalent thermal conductivity can be obtained as Equations 1, 2.

$$K_{eq,z} = \frac{\beta K_1 + K_2}{1+\beta} \tag{1}$$

$$K_{eq,x,y} = \frac{K_2(\beta K_1 + K_2)\sqrt{\pi/\beta + \pi}}{2K_2(1+\beta) + (\beta K_1 + K_2)\left(\sqrt{\pi/\beta + \pi} - 2\right)} \tag{2}$$

Where $K_{eq,z}$ and $K_{eq,x,y}$ are the equivalent thermal conductivity coefficients in the z-direction and x-y direction respectively. K_1 and K_2 are the thermal conductivity coefficients of TSV (Cu) and Si respectively, and β is the volume ratio of Cu to Si.

For the elastic modulus and thermal expansion coefficient, the finite element method is used to extract their equivalent parameters. Taking the TSV unit model (Figure 1A) as an example, a uniaxial tensile simulation is performed. A fixed constraint is applied to one side of the hexahedral unit, and a small displacement is applied to the opposite side. The support reaction force and stress strain of the unit can be obtained through finite element simulation. The equivalent Young's Modulus and Poisson's ratio of the unit is calculated using Equations 3–5.

$$E_z = \frac{\sigma_z}{\varepsilon_z} = \frac{F_z}{A_z \cdot \varepsilon_z} \tag{3}$$

$$E_{x,y} = \frac{\sigma_x}{\varepsilon_x} = \frac{F_x}{A_x \cdot \varepsilon_z} \tag{4}$$

$$\nu_{x-y} = \left|\frac{\varepsilon_y}{\varepsilon_x}\right| \tag{5}$$

Where E_z and $E_{x,y}$ are the equivalent elastic moduli in the z and x-y directions respectively, $\nu_{x\text{-}y}$ is the equivalent Poisson's ratio, σ_z and σ_x represents the stress in the z and x directions respectively, ε_z and $\varepsilon_{x,y}$ are the tensile strains in the z and x directions (or y directions), and F_z and F_x are the support forces in the z and x directions respectively. A_x and A_z are the cross-sectional areas of the unit model parallel to the x and z directions respectively.

The method for obtaining the equivalent coefficient of thermal expansion is as follows: set the normal degrees of freedom of the three adjacent surfaces of the model to 0, and set the temperature rise of ΔT, as shown in Figure 1B. The thermal expansion coefficient of the model is obtained from Equations 6, 7.

$$\alpha_{x,y} = \frac{\varepsilon_x^T}{\Delta T} \tag{6}$$

$$\alpha_z = \frac{\varepsilon_z^T}{\Delta T} \tag{7}$$

Where $\alpha_{x,y}$ and α_z are the thermal expansion coefficients in the x-y and z directions respectively, and ε_x^T and ε_z^T are the thermal strains in the x and z directions respectively.

The calculation process for density and specific heat capacity is relatively simple. According to the definition of

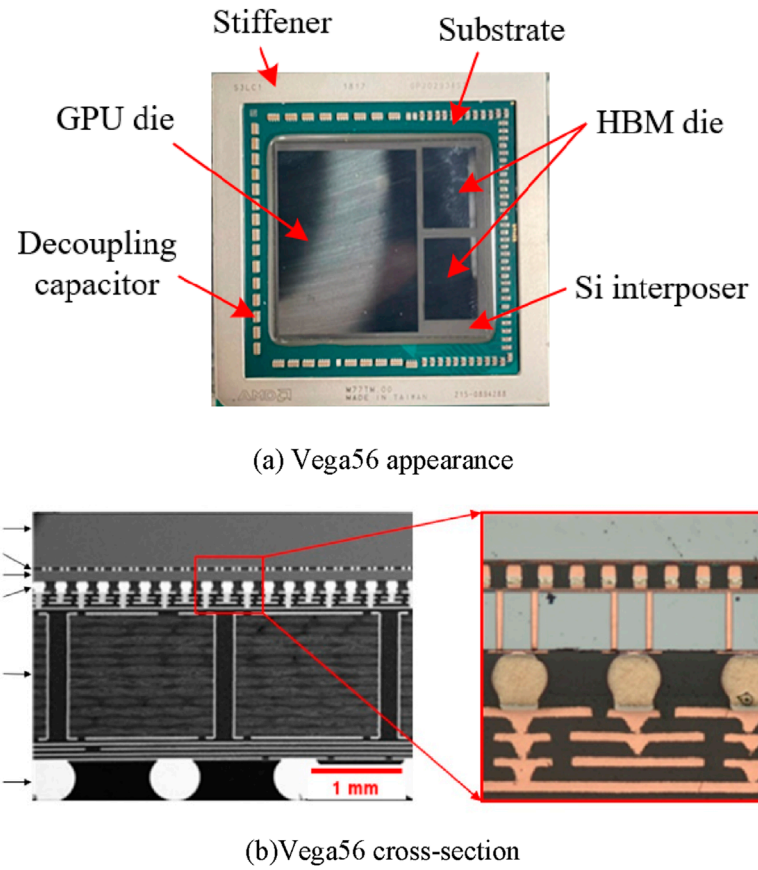


FIGURE 2
Vega56 appearance and cross-section. **(A)** Vega56 appearance. **(B)** Vega56 cross-section.

TABLE 1 Dimensions of Vega56.

Part	Dimensions (length × width × height/diameter × height, mm)
GPU	26.20 × 19.62 × 0.78
HBM	12.08 × 7.78 × 0.76
Si interposer	30.00 × 27.68 × 0.1
CPB	0.024 × 0.04 (pitch: 0.054)
TSV	0.01 × 0.1 (short pitch: 0.06; long pitch: 0.192)
C4 bumps	0.1 × 0.095 (pitch: 0.192)
Substrate	47.5 × 47.5 × 1.64
Stiffener	47.08 × 4.20 × 0.57

density shown in Equation 8.

$$\rho_{eq} = \frac{m}{V} = \frac{m_{Si} + m_{Cu}}{V_{Si} + V_{Cu}} = \frac{\rho_{Si} V_{Si} + \rho_{Cu} V_{Cu}}{V_{Si} + V_{Cu}} \tag{8}$$

Where ρ_{eq} is equivalent density, ρ_{si} and ρ_{cu} are density of Si and Cu respectively. Introducing the volume ratio $\beta = \frac{V_{Cu}}{V_{Si}}$, the Equation 8 can be simplified to Equation 9.

$$\rho_{eq} = \frac{\rho_{Si} + \rho_{Cu}\beta}{1 + \beta} \tag{9}$$

Similarly, the formula for calculating the equivalent specific heat capacity can be obtained as Equation 10.

$$C_{eq} = \frac{\Delta Q}{m\Delta T} = \frac{C_{Si} m_{Si} \Delta T + C_{Cu} m_{Cu} \Delta T}{m\Delta T} = \frac{C_{Si}\rho_{Si} + C_{Cu}\rho_{Cu}\beta}{\rho_{eq}(1+\beta)} \tag{10}$$

Where C_{eq} is equivalent specific heat capacity, C_{Si} and C_{cu} are heat capacity of Si and Cu respectively.

2.2 Simplified model thermal simulation

In this paper, the Vega56 graphics card core, a representative 2.5D package manufactured by Advanced Micro Devices (AMD), has been meticulously chosen as the subject of study. Vega56 contains a graphics processing unit (GPU) die and two high bandwidth memory (HBM) dies. The three dies are interconnected with the Si interposer through CPBs. The Si interposer is interconnected with the substrate through C4 bumps, and the

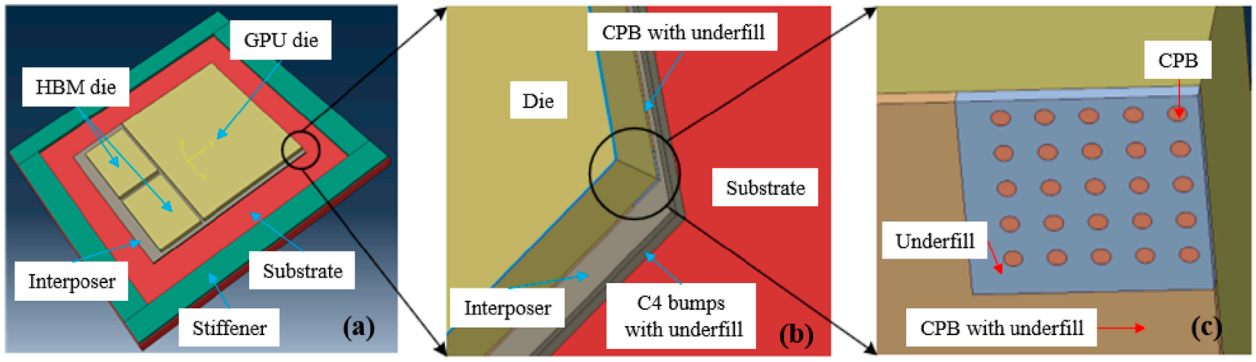


FIGURE 3
Simulation model of Vega56: **(A)** is overall view of the model; **(B)** shows the simplified model of interposer, C4 bumps with underfill and CPB with underfill; **(C)** shows the simplified model at corner of chip.

TABLE 2 Material parameters.

Material	E (Gpa)	ρ (g/cm^3)	α (1 × 10^{-6}/°C)	ν	C (W/(m×°C))
Cu	110	8.93	16.4	0.343	Table 3
Si	112.4	2.329	2.49	0.28	Table 3
Aluminum alloy	70.2	2.82	23.2	0.3	236.34
Substrate	18.75	2.44	10.2	0.12	16.5
Underfill	43.25	7.4	28.2	0.363	64.2
SAC305	54	7.38	40	0.363	50.3
Pb37Sn63	32.62	8.4	2.54	0.363	50
Interposers	E_Z:110.25 E_{xy}:110.529	2.395	$\alpha_{x,y}$:3.721 α_z:3.654	0.292	Table 3
C4 bumps with underfill	E_Z:40.05 E_{xy}:41.12	7.89	$\alpha_{x,y}$:2.52 α_z:2.51	0.363	$K_{eq,z}$:61.56 $K_{eq,xy}$:60.34
CPB with underfill	*Ez*:89.64 *Exy*:93.45	8.12	$\alpha_{x,y}$:4.89 α_z:4.57	3.592	$K_{eq,z}$:89.58 $K_{eq,xy}$:84.21

TABLE 3 Partial material thermal conductivity.

Material		C (W/(m·°C))			
		−55°C	0°C	25°C	165°C
Cu		431.8	401	398	389.9
Si		62.9	79.5	85.9	121.6
Interposers	$K_{eq,z}$	77.6	92.3	98.3	132.3
	$K_{eq,xy}$	53.8	67.3	72.6	101.8

substrate is connected to the computer motherboard through BGA solder balls. Its appearance is shown in Figure 2A, and its cross-section is shown in Figure 2B.

ABAQUS was used to conduct thermal simulation analysis of the model. The dimensions of each part of Vega56 are shown in Table 1. In light of the substantial quantity of CPBs, the construction of all individual CPBs would lead to exceedingly intricate models that demand considerable computational resources. In the thermal cycle, the dangerous solder joints of the chip are located at the center and corners, while the rest of the solder joints are relatively safe. Therefore, when constructing the model of CPBs in this paper, only the CPBs at the center of the chip and the four corners of the chip were constructed, and the rest was simplified using the equivalent model. In addition, the substrate, C4 bumps layer, and Si interposers were also simplified into rectangular shapes, resulting in the simulation model shown in Figure 3.

Based on the size and pitch of C4 bumps, CPBs, and TSVs, the volume ratio β could be calculated to be 20.532%, 15.514%, and 3.409%. Through (1)–(10), the material parameters of each structure

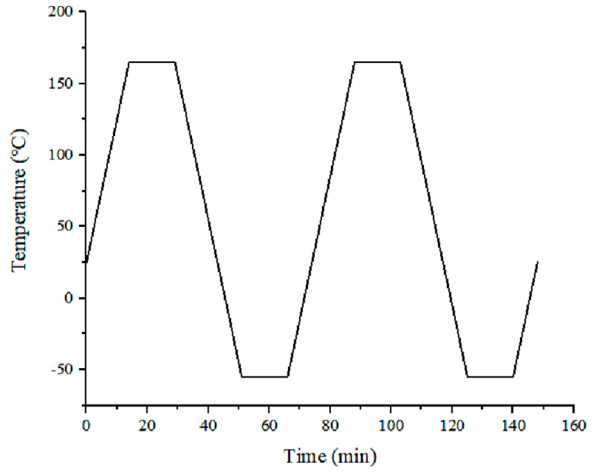


FIGURE 4
Thermal cycle curve.

in the model could be obtained, as shown in Table 2. The thermal conductivity of Cu, Si, and Interposers is temperature dependent, as shown in Table 3.

The simulation conditions for thermal cycling were −55°C~165°C, with a temperature change rate of 10°C/min, a temperature retention time of 15 min, and a cycle period of 74 min. In the thermal cycling simulation, the initial temperature was set to 25°C, with a cycle time of 2 h per cycle, culminating in a total duration of 148 min for the thermal cycling regimen. The thermal cycle profile is illustrated in Figure 4. During the static analysis segment, the boundary conditions were meticulously defined to incorporate fixed restraints at the vertices of the substrate's basal plane.

Eight-node hexahedral solid elements were used for meshing. During the transient thermal analysis, the DC3D8 unit was used, and during the static analysis the C3D8R unit was used. For thin-layer structures, the number of meshes in the z direction was controlled to two layers of meshes at least. The meshing results are shown in Figure 5.

The temperature field obtained from transient thermal simulation was put into static simulation as a predefined field to obtain the stress changes and warping deformation of the device under temperature cycling. The simulation results are shown in Figures 6A, B.

It could be seen that during the heating stage, the chip mainly experienced arching warpage, while during the cooling stage, concave warpage occurred. At the maximum temperature, the warpage was the largest, reaching 44.717 μm. At the minimum temperature, the maximum concave warpage value was −24.075 μm. Figure 6C shows the variation of the maximum warpage over time within a cycle, which was similar to the temperature change. From the GPU stress distribution, it could be seen that the maximum stress point was located at the corners, mainly due to the smaller thermal expansion coefficient of the silicon chip and the larger thermal expansion coefficient of the substrate. Therefore, the warpage stress on the GPU was mainly caused by the warping of the substrate.

2.3 Verification of simulation

Shadow moire interferometry (Zhu et al., 2018; Du et al., 2019; Yeh et al., 2019) is a non-contact optical technology for warpage full-field measurement. It uses interference between a reference grating and its shadow on the sample to measure the relative vertical displacement of each pixel position. This technology was used for experimental verification of the overall model in this paper.

The equipment used in this article is TherMoire AXP produced by akrometrix, as shown in Figure 7A. The sample was heated using infrared heating, and was fixed on a standard glass block with an ultra-low coefficient of thermal expansion (CTE). The bending radius of the standard glass is known, which can be used to calibrate the influence of the external environment during the experiment. A thermocouple was installed next to the sample to detect temperature changes in the sample. The experimental setup is shown in Figure 7B.

In order to maintain the device warpage in a steady state during experimentation, a heating rate of 10°C per minute was established, while the cooling rate was controlled to remain below −10°C per minute. The experimental setup included a maximum temperature of 165°C, with an ambient condition set at 25°C. Thermocouples were used to detect the surface temperature of the device in real time, and the temperature change curve was obtained as shown in Figure 8A.

During the experiment, the surface warpage of the sample was measured every 10 °C. Each measurement used the built-in three-step phase shift method of the equipment to obtain the surface warpage value. The experimental results are shown in Figure 8B.

The sample already had a warpage of 14 μm before heating, which perhaps caused by reflow soldering process. From Figure 8B, it could be seen that the initial warpage was arching warpage, that is, the center of the sample was higher than the four corners. As the temperature increases, the sample's arching warpage further intensified, and when the maximum temperature was reached, the warpage value increased to a maximum of 56 μm. As the temperature decreases, the warpage value gradually decreased and eventually returned to the initial warpage value.

The temperature change curve obtained from the experiment was input to the previous simulation model as a boundary condition, and the warpage of the device surface was obtained, as shown in Figure 8B. The simulation results were in good agreement with the relative warpage measured in the experiment. The error at the maximum warpage was 6.47%, and the maximum error does not exceed 20%, with an average error of 8.93%. This indicates that the simplified modeling and simulation methods used in this paper have sufficient accuracy.

3 Simulation of fatigue crack propagation of CPB

3.1 Boundary load curve extraction

In the process of model refinement, the specific CPB located in close proximity to the apex of stress concentration within the overall model was precisely delineated. Subsequently, a detailed submodel

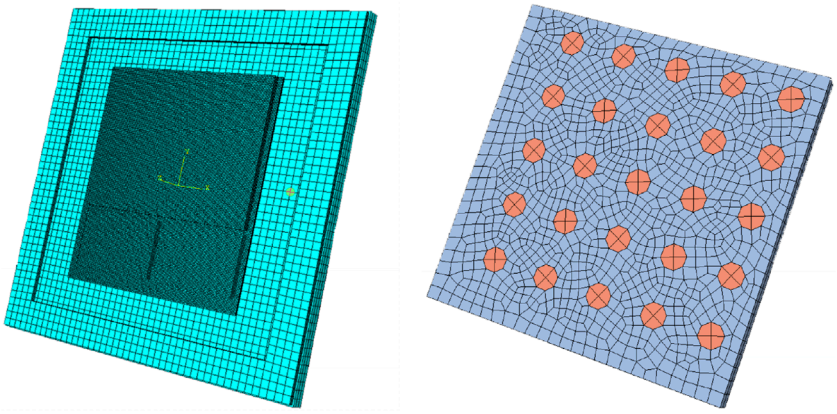


FIGURE 5
Meshing results of Vega56. **(A)** Overall model. **(B)** CPB.

encompassing this region of interest was extracted and delineated, as illustrated in Figure 9.

The solder layer material is SAC305, which is a viscoplastic material. Under thermal cycle conditions, plastic deformation and creep deformation mainly occur. The plastic constitutive model of SAC305 is shown in Equation 11.

$$\sigma = C_p \varepsilon_p^{n_p} \tag{11}$$

where ε_p is equivalent plastic strain, C_p and n_p are both time-dependent material parameters (Cheng et al., 2008), as show in Table 4.

The steady-state creep constitutive model is a hyperbolic sine creep constitutive model (Glane et al., 2023) as Equation 12.

$$\dot{\varepsilon} = C[\sinh(\alpha\sigma)]^n \exp\left(-\frac{Q}{kT}\right) \tag{12}$$

where Q is creep activation energy, T is temperature, n is stress exponent, k is Boltzmann constant, σ is applied stress, C and α are material constant, and $\dot{\varepsilon}$ is steady state creep strain rate. The relevant material parameters are shown in Table 4, and other material parameters are shown in Table 5.

Set the boundary conditions of the submodel as the displacement simulation results of the upper and lower surfaces. The boundary conditions for the submodel were established utilizing the displacement simulation outcomes obtained from the upper and lower surfaces. To achieve stable viscoplastic flow of the solder, the boundary conditions were cyclically loaded. The equivalent stress of the CPB was extracted for each cycle, with the stabilized equivalent stress serving as the boundary stress for subsequent analysis. Since the stress on the CPBs was mainly caused by the deformation of the dies, the external force was mainly on the upper and lower surfaces. The stress on the copper pillar was mainly in the *z*-axis direction, while the stress in the *x* and *y* directions was smaller. Consequently, in the simulation of fatigue crack propagation, the stress acting in the *x* and *y* directions was deemed negligible. The curve of the average principal stress on the outer surface of the copper pillar over time is shown in Figure 10.

3.2 Thermal fatigue crack propagation simulation

Under the influence of temperature, due to the expansion movement of atoms, two intermetallic compounds, Cu_6Sn_5 and Cu_3Sn, will gradually form between the solder and the copper pillar (Roy et al., 2022; Arafat et al., 2020). Generally speaking, the growth rate of Cu_6Sn_5 is greater than that of Cu_3Sn, so Cu_6Sn_5 is prone to forming undulating wave shapes, while Cu_3Sn generally forms relatively flat elongated shapes (An and Qin, 2016).

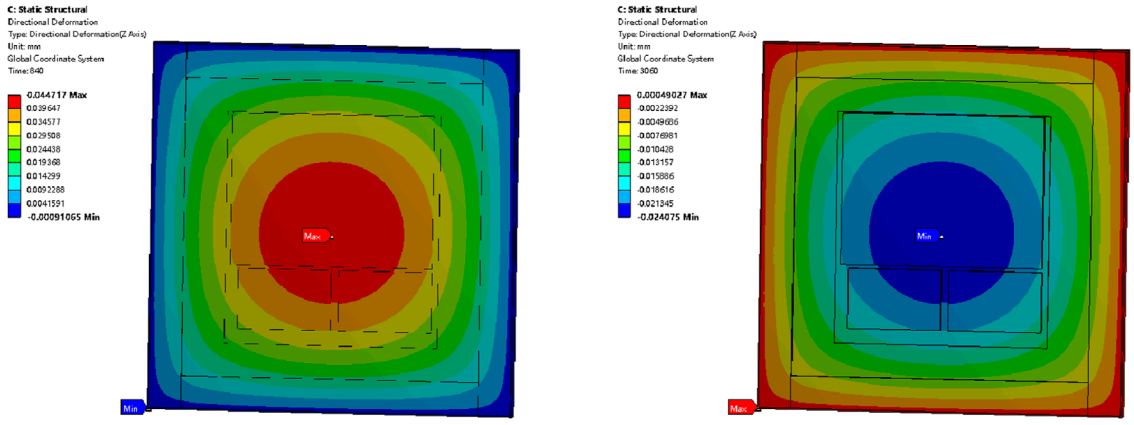
The IMC layer morphology characteristic parameters set in this paper are shown in Table 6. R_{rms} is the roughness of IMC layer, d_{ave} is the average thickness, λ_{ave} is the average distance between wave paeks.

Utilizing the MATLAB computational environment, a one-dimensional Gaussian random rough surface was meticulously modeled, with the explicit aim of synthesizing a stochastic rough surface profile that rigorously adhered to the specified parameters delineated within Table 6. Then, the rough surface data was imported into the CPB model, as shown in Figure 11A. During the crack propagation process, the CPE4R unit was used for simulation calculations. This unit can handle complex stress states and provide relatively high computational efficiency. The meshes are shown in Figure 11B.

According to the research in Li et al. (2020), there are two main ways of crack expansion in CPBs. Mode 1 is the crack propagation in SAC305, and Mode 2 is the crack propagation in Cu_6Sn_5, as shown in Figure 12.

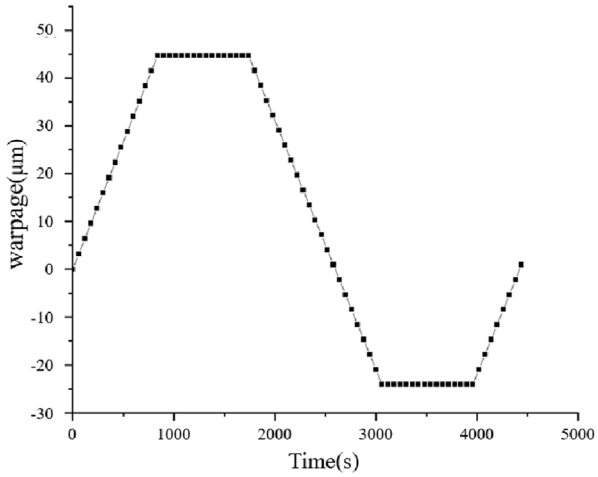
Two initial cracks with length a0 = 0.5 μm were constructed respectively. The first initial crack was located in SAC305 and was a horizontal crack used to simulate Mode 1. The second initial crack was set at the interface between SAC305 and Cu_6Sn_5, with an inclination angle of 60°, to simulate Mode 2. The constructed simulation models are shown in Figures 11C, D.

Crack propagation can be roughly divided into three stages: crack initiation stage, stable propagation stage, and unstable propagation stage. The crack propagation rate during the stable



(a) Warpage distribution at maximum temperature

(b) Warpage distribution at minimum temperature



(c) Variation of the maximum warpage over time

FIGURE 6
Warpage distribution and variation. **(A)** Warpage distribution at maximum temperature. **(B)** Warpage distribution at minimum temperature. **(C)** Variation of the maximum warpage over time.

propagation stage can be described using the Pairs formula (Rajaguru et al., 2019) as Equation 13.

$$\frac{da}{dN} = C(\Delta K)^m \tag{13}$$

where da/dN is the crack propagation rate; C and m are constants, which can be obtained by fitting experimental data; ΔK is the stress intensity factor amplitude.

The boundary load curve, as illustrated in Figure 10, was input into the model. The simulation of fatigue cracks was conducted through the direct cycle analysis step within the Abaqus software. Furthermore, the model parameters of the Paris formula was input, ensuring a comprehensive analysis of the fatigue crack propagation under the specified loading conditions. The parameters C and m in the Paris formula were obtained by fitting the experimental data in Tian et al. (2017), and the values of C and m are shown in Equation 14.

$$\begin{cases} \log C = -7.8 \\ n = 2.7 \end{cases} \tag{14}$$

The fatigue crack propagation results of Mode 1 and Mode 2 are shown in Figure 13. And the relationship curve between the crack length a and the number of cycle N in Mode 1 and Mode 2 were established, as shown in Figure 14. In the crack propagation of Mode 1, as depicted in Figure 13A, the crack initiates from an initial flaw and propagates in a direction parallel to the upper surface of the CPB solder layer. This propagation continues until the crack traverses the entire solder layer, which is in close agreement with the Mode 1 crack propagation path for CPB as shown in Figure 12A.

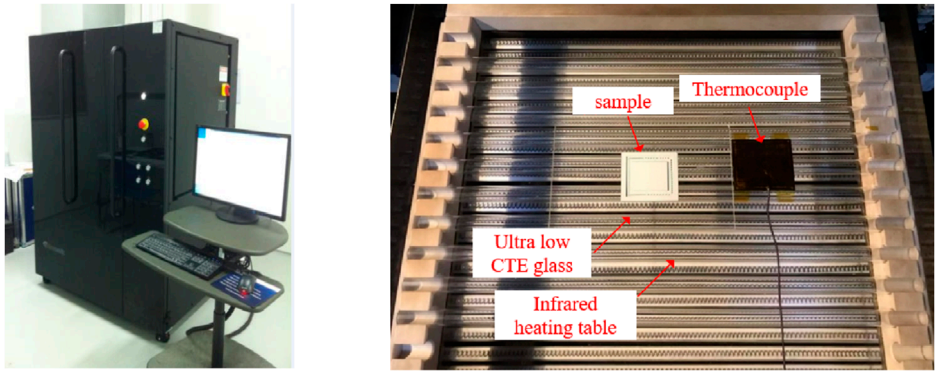


FIGURE 7
Equipment and experimental setup. **(A)** TherMoire AXP. **(B)** Shadow moire interferometer heating platform.

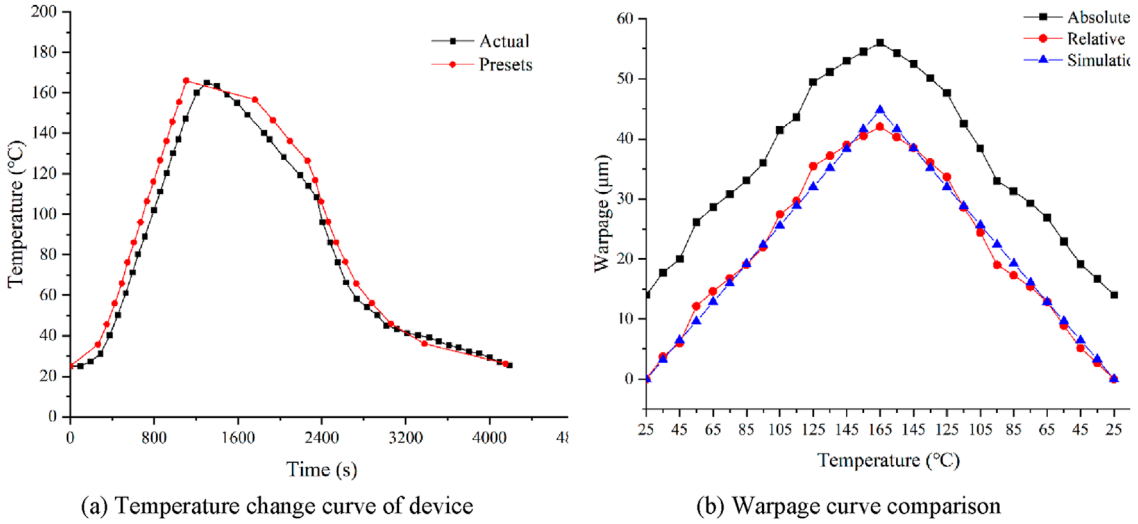


FIGURE 8
Temperature change curve and warpage curve comparison in the Verification experiment **(A)** Temperature change curve of device. **(B)** Warpage curve comparison.

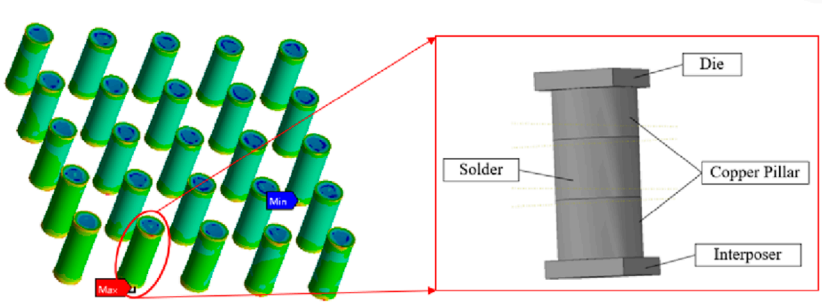


FIGURE 9
CPB submodel.

TABLE 4 Plastic and creep parameters of SAC305.

Material	Plastic parameters		Creep parameters			
SAC305	C_p	n_p	C	α	n	Q/k
	121.6–0.4 × T (°C)	0.29–0.00046 × T (°C)	441,000	0.005	4.2	5,412

TABLE 5 Other material parameters.

Material	P (g/cm^3)	E (Gpa)	ν	CTE (1 × 10^{-6}/°C)	C (W/(m×°C))
SAC305	7.38	54	0.363	28.2	50.3
Cu6Sn5	7.96	129.01	0.3	21.3	78.6
Cu3Sn	8.12	144.50	0.28	18.6	87.3

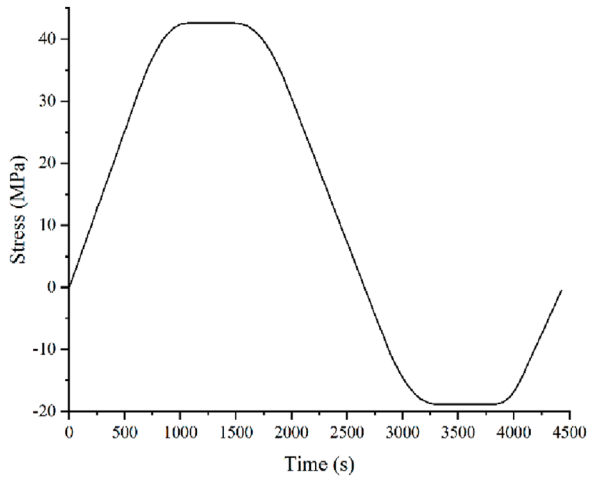


FIGURE 10
CPB boundary stress.

TABLE 6 Morphological characteristics of IMC layer.

Material	R_{rms} (Ra)	d_{ave} (μm)	λ_{ave} (μm)
Cu_6Sn_5	0.95	5.3	2.32
Cu_3Sn	0.53	1.97	4.56

This behavior is likely attributed to creep damage in the solder layer proximate to the upper copper pillar. In contrast, for Mode 2 crack propagation, as illustrated in Figure 13B, the initial crack is situated near the IMC layer within the solder. The crack then crosses the interface between the SAC305 solder and the IMC layer, entering the Cu_6Sn_5 phase and propagating parallel to the lower surface of the copper pillar. This propagation continues until the crack laterally spans the entire IMC layer, closely aligning with the Mode 2 crack propagation path depicted in Figure 12B. Moreover, the crack propagation rate for Mode 2 was observed to be faster than that for Mode 1.

3.3 Fatigue lifetime prediction

The fatigue crack propagation life is the number of cycles that a crack undergoes from the initial length a_0 to the critical length a_c. The critical length a_c is closely related to the stress intensity factor K at the crack tip and the fracture toughness K_C of the material. When $K \geq K_C$, the crack will experience unstable propagation and quickly reach the life limit of the structure (Wang et al., 2023; Alter et al., 2020). The unstable propagation of cracks can be determined by Equation 15, 16.

$$K_{\max} = f\sigma_{\max}\sqrt{\pi a_C} \leq K_C \tag{15}$$

$$a_C = \frac{1}{\pi}\left(\frac{K_C}{f\sigma_{max}}\right)^2 \tag{16}$$

where f is the geometric correction coefficient, and σ_{max} is the maximum value of applied stress.

In this paper, f is 1.121, σ_{max} is 43.13 MPa, and the fracture toughness of Cu_6Sn_5 is 0.481 MPa·m$^{1/2}$ (Ghosh, 2004). The critical length of Mode 2 could be determined to be 21.78 μm. From the a-N curve in Figure 14, it could be concluded that the fatigue lifetime of Mode 2 is 1,470 cycles. When the number of cycles in Mode 1 reached 1900, the crack almost penetrated the entire CPB, indicating a fatigue lifetime of 1900 cycles.

4 Discussion

From the lifetime prediction results of Mode 1 and Mode 2, it could be seen that when the crack propagated in the IMC layer, the fatigue lifetime of CPB was shorter than that of the crack located in the solder, and the difference between the two was significant $\delta=(N_1-N_2)/N_1 \times 100\% = 22.63\%$. This indicated that IMC had a significant influence on the fatigue lifetime of CPBs.

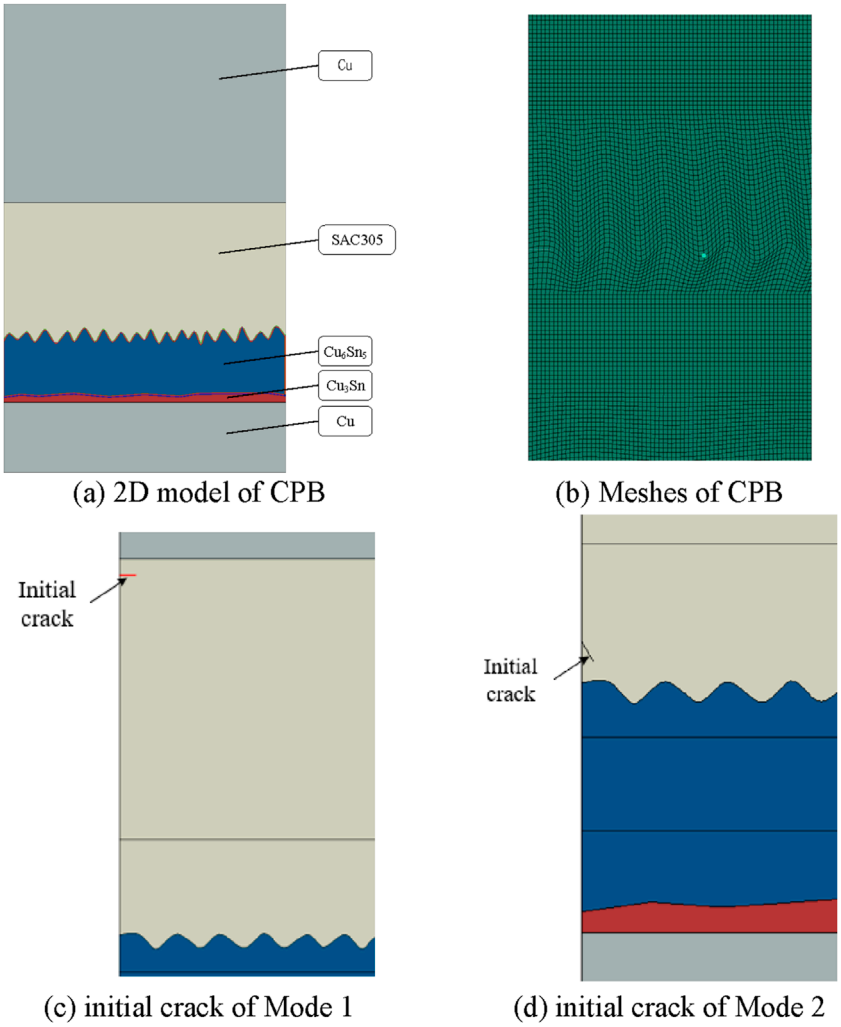


FIGURE 11
2D model and Meshes of CPB and initial crack simulation model. **(A)** 2D model of CPB **(B)** Meshes of CPB **(C)** initial crack of Mode 1**(D)** initial crack of Mode 2.

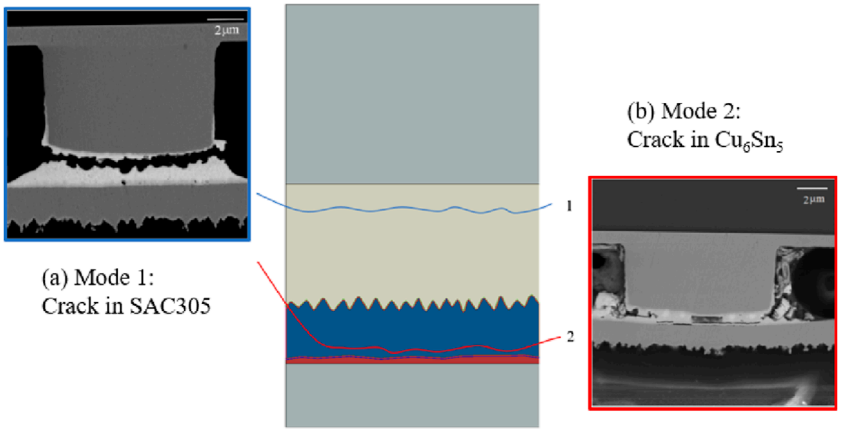


FIGURE 12
Schematic diagram of crack propagation: **(A)** Mode 1 crack is located in SAC305; **(B)** Mode 2 crack is located in Cu_6Sn_5 (Li et al., 2020).

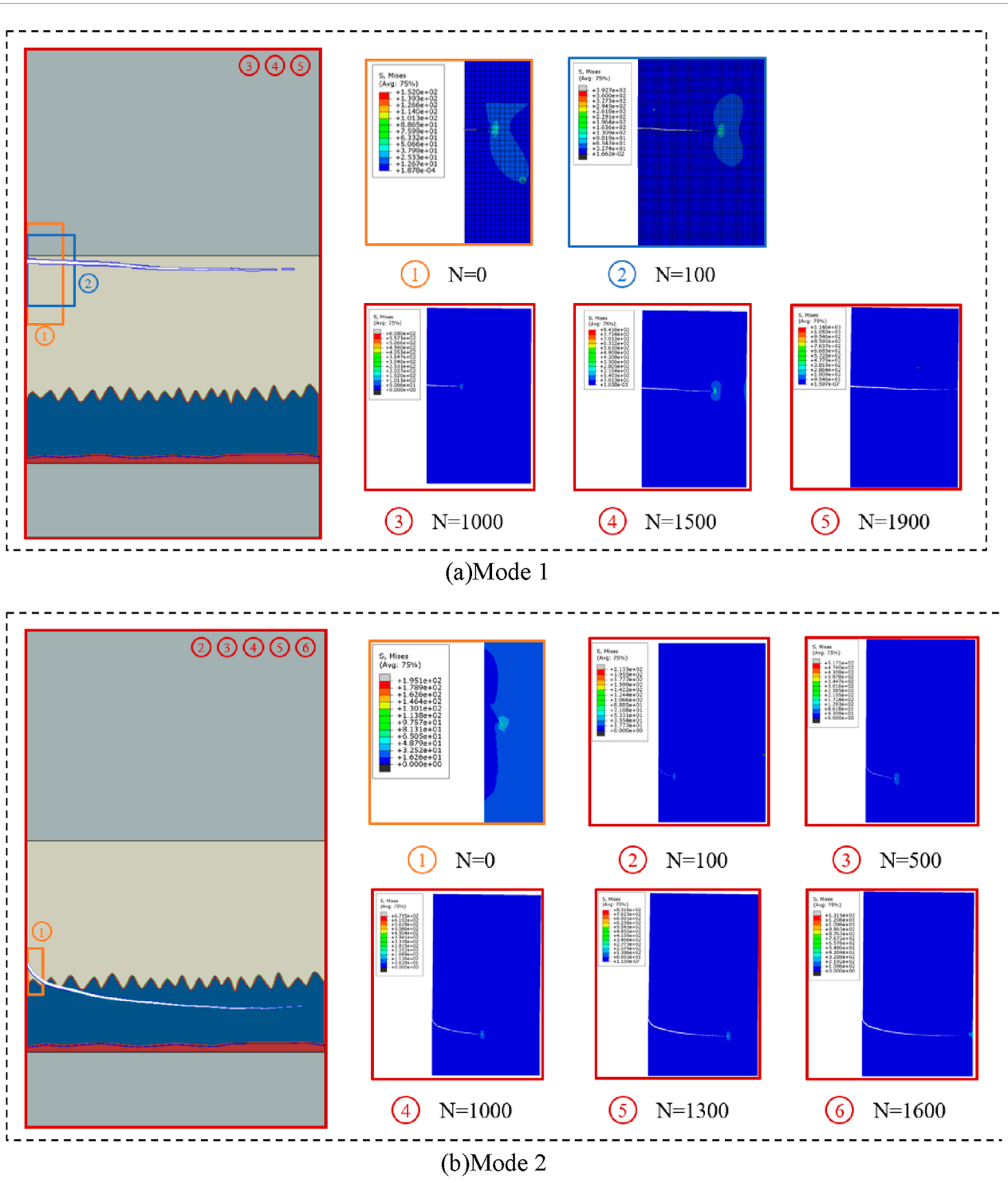


FIGURE 13
Fatigue crack propagation path of Mode 1 and Mode 2. **(A)** Mode 1. **(B)** Mode 2.

To investigate the effect of IMC layer thickness on the fatigue life of CPBs, this paper constructed simulation models with different IMC layer thicknesses. Due to the significant impact of the IMC layer, only the fatigue lifetime of Mode 2 was simulated. The a-N curves of CPBs with different IMC layer thicknesses are shown in Figure 15. And the fatigue lifetime prediction results of CPBs with different IMC layer thicknesses are shown in Table 7.

From Figure 15, it can be seen that as the thickness of the IMC layer increased, the shape of the a-N curve remained basically unchanged, but the rate of crack propagation increased rapidly. It can also be seen from the lifetime prediction results that as the IMC increased, the fatigue lifetime of CPB will decrease significantly. When all the solder layers were converted to IMC, its fatigue lifetime decreased from 1,470 cycles to 825 cycles, a decrease of 43.88%.

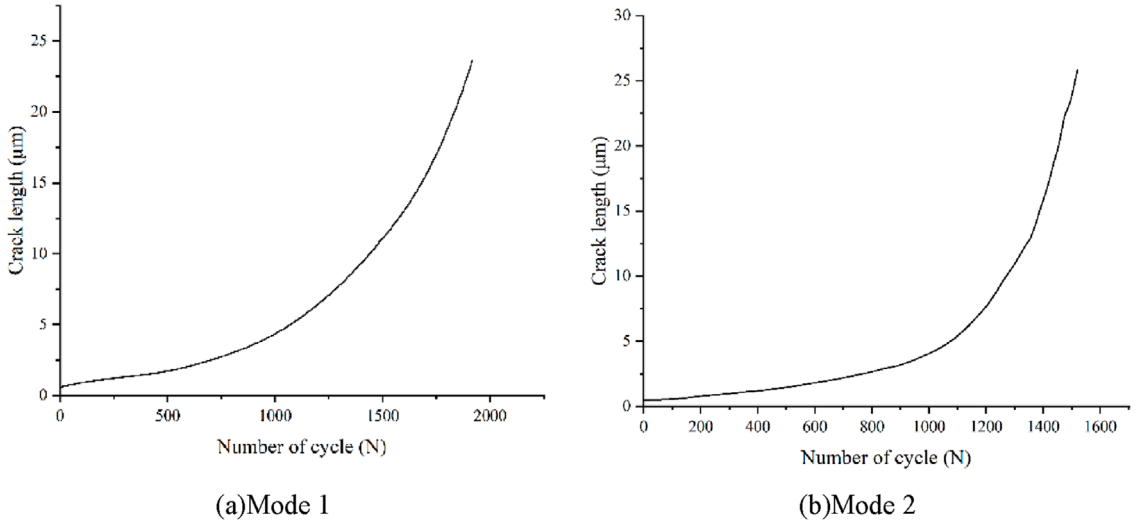


FIGURE 14
A–N curve of Mode 1 and Mode 2. **(A)** Mode 1. **(B)** Mode 2.

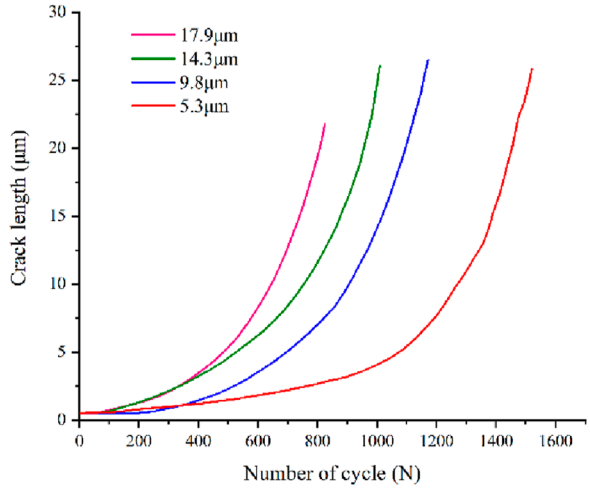


FIGURE 15
a-N curves of CPB with different IMC layer thicknesses.

TABLE 7 Fatigue lifetime of CPBs with different IMC layer thicknesses.

IMC layer thicknesses (μm)	5.3	9.8	14.3	17.9
Fatigue lifetime (cycle)	1,470	1,119	977	825

These results indicate that the existence of the IMC layer accelerates the fatigue crack propagation of CPB, which will seriously reduce the fatigue lifetime of CPB, and the thickness of the IMC layer is one of the key influencing factors. Therefore, in the preparation process of CPB, it is necessary to choose appropriate process parameters to ensure that the IMC layer is thin, and attention should also be paid to the growth of the IMC during service.

5 Conclusion

This paper takes the CPBs in 2.5D package as the research object, and establishes a method for obtaining the lifetime of CPBs based on the basic theory of fatigue crack propagation. Using the extended finite element simulation method, the fatigue lifetime of CPBs with different IMC layer thicknesses under thermal cycling was simulated, and the influence of IMC layer thickness on the fatigue lifetime of CPBs was analyzed. Through the simulation results of fatigue crack propagation at CPBs, it was found that when the crack propagated in IMC, the fatigue lifetime of CPB was smaller than the lifetime when the crack propagated in the solder layer. This indicates that the influence of IMC layer on the fatigue lifetime of CPB is significant. And as the thickness of the IMC layer increases, the fatigue lifetime of the CPBs also significantly decreases. When the thickness of the IMC layer reaches 100% of the solder layer height, the fatigue lifetime of CPB will decrease by 43.88%. Therefore, when predicting the lifetime of the CPBs, it is necessary to consider the impact of the IMC layer. In addition, there may be defects such as voids in the IMC layer of CPBs, which have a certain impact on predicting crack propagation lifetime. In future research, initial defects can be incorporated into simulations to establish more accurate lifetime prediction methods.

Data availability statement

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation.

Author contributions

YZ: Conceptualization, Investigation, Methodology, Writing–review and editing. QL: Data curation, Software,

Validation, Writing–original draft, Writing–review and editing. TM: Data curation, Formal Analysis, Validation, Writing–review and editing. SL: Data curation, Software, Writing–review and editing. XZ: Data curation, Software, Writing–review and editing.

Funding

The author(s) declare that no financial support was received for the research, authorship, and/or publication of this article.

Acknowledgments

We would like to thank the Reviewers for their suggestions which have resulted in substantial improvement to the quality of this manuscript.

Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Publisher's note

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frontiers | Frontiers in Materials

TYPE Review
PUBLISHED 24 December 2024
DOI 10.3389/fmats.2024.1532859

OPEN ACCESS

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RECEIVED 22 November 2024
ACCEPTED 09 December 2024
PUBLISHED 24 December 2024

CITATION
Zhou Z, Lang F, Farlim V, Zhang Z, Li S and Dong R (2024) Review on multi-scale mechanics fundamentals and numerical methods for electronics packaging interconnect materials.
Front. Mater. 11:1532859.
doi: 10.3389/fmats.2024.1532859

Review on multi-scale mechanics fundamentals and numerical methods for electronics packaging interconnect materials

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This paper examines multiscale theories and numerical methods for interconnect materials in electronic packaging, focusing on the interplay among micro-scale morphology, meso-scale structure, and macro-scale behavior to improve material reliability and performance prediction. It reviews advanced materials, such as sintered silver and lead-free solder, alongside methodologies like Molecular Dynamics (MD) simulations, cohesive modeling, crystal plasticity modeling, and phase-field modeling, to evaluate mechanical and thermal properties across scales and their long-term reliability. At the microscopic scale, MD simulations reveal the influence of atomic arrangements, grain orientations, and dislocation evolution on mechanical behavior. At the mesoscopic scale, phase-field and crystal plasticity models are combined to analyze pore evolution, grain sliding, and stress concentration under thermal cycling. Macroscopically, models like Anand and Unified Creep Plasticity (UCP) describe viscoplasticity, creep, and fatigue life, offering insights into performance under complex conditions. By systematically integrating diverse research methods and theoretical models, this review highlights the applicability of a multiscale coupling framework, providing a comprehensive understanding of the correlations between morphology, structure, and behavior. This framework serves as theoretical guidance for developing innovative packaging solutions and optimizing materials for high-density, low-power electronic devices.

KEYWORDS

multi-scale mechanics, electronics packaging, interconnect materials, finite element analysis, reliability analysis

1 Introduction

The rapid advancement of electronics necessitates miniaturization and high-density integration in packaging. Technologies like Wafer-Level Packaging (WLP) (Elshabini et al., 2006), System-in-Package (SiP) (Fontanelli, 2008; Dai, 2016; Wang et al., 2023), and heterogeneous integration (Lee et al., 2020; Lau, 2022) address these needs. Notably, 3D heterogeneous integration bridges chip-level and system-level

integration (Choudhury, 2010; Zhang et al., 2022). However, complex materials and micro-scale morphology demand multi-scale investigation into performance and reliability.

As devices shrink, mechanical properties like conductivity and thermal expansion become critical. Traditional materials fall short of modern packaging demands. Research focuses on nanomaterials, sintered silver and copper, and lead-free solder to meet high-density packaging requirements (Paknejad and Mannan, 2017; Zhang et al., 2019; Aamir et al., 2020). Nanoindentation evaluates stress-strain relationships (Long et al., 2021b). While sintered silver offers reliability, it's costly; thus, sintered copper is explored as a cost-effective alternative (Chen and Siow, 2021). Models study solder deformation and failure over time. Finite Element Analysis (FEA) efficiently assesses performance (Mathew et al., 2021; Gharaibeh and Wilde, 2023). Life prediction models like Coffin-Manson and Basquin are widely used (Tan et al., 2014; Chen et al., 2020; Coffin, 2022; Mathew et al., 2022). These models predict lifespan under cyclic loading, evaluating long-term reliability. Therefore, solder fatigue behavior and failure mechanisms are crucial in macroscopic modeling.

However, macroscopic models cannot fully describe solder properties due to micro- and meso-scale influences. Behaviors like void formation and grain orientation changes affect reliability. Simulations focusing on these scales are key (Lederer et al., 2021; Long et al., 2022), providing insights into porosity effects and guiding design improvements (Ma et al., 2023; Long et al., 2023c). Advances in Molecular Dynamics (MD) and Crystal Plasticity Finite Element Method (CPFEM) are pivotal for understanding these correlations.

This paper explores cross-scale theoretical research on packaging materials, focusing on relationships between micro-scale morphology, meso-scale structure, and macro-scale behavior. It analyzes mechanical behavior and reliability using integrated simulations. MD and Monte Carlo simulations reveal atomic-level details; meso-scale analysis employs crystal plasticity and phase-field methods; macroscopic models like Anand and UCP describe viscoplasticity and creep. Long-term performance evaluation uses SEM and FEM to support life prediction. The proposed multiscale framework spans microscopic to macroscopic scales and transient to long-term behavior, providing a foundation for material development and optimization. It guides simulation and verification of micro-scale morphology and advanced designs, offering new insights and practical guidance for material optimization in electronic packaging.

2 Electronics interconnection materials and its morphologies

In electronic packaging, micro-scale morphology of solders significantly influences performance and stability. SnPb solder and Sn-Ag-Cu (SAC) lead-free solder exhibit unique characteristics. Siviour et al. (2005) observed tin-rich regions appearing dark and lead-rich regions light in SnPb solder, indicating compositional differences. Figure 1A presents a cross-sectional SEM image showing the overall morphology of SnPb solder on copper. Tu and Zheng (2001) noted that a continuous Cu_6Sn_5 layer forms at the SnPb solder interface, thickening over time and developing into columnar grains (Figures 1B, C). Zhang et al. (2007) found that on a copper substrate, the Cu_6Sn_5 layer has a scallop-like shape, while the Cu_3Sn layer is flat. As soldering continues, the intermetallic compound (IMC) layer thickens and forms a complex multilayer structure.

For SAC lead-free solder, Aamir et al. (2020) observed homogeneously distributed Ag_3Sn and Cu_6Sn_5 IMCs within the β-Sn matrix; adding trace elements like Ti and Fe refines grains and enhances structure. Aamir et al. (2017) noted that thermal aging causes IMC coarsening and structural inhomogeneity, but La doping mitigates these effects. Gain and Zhang (2019) found that SAC305 solder contains uniformly distributed Ag_3Sn and Cu_6Sn_5 IMC particles with Sn matrix grains measuring 20–30 μm. Figure 1D presents the EBSD image of as-cast SAC305 alloy, showing that high temperature and humidity cause significant growth of IMCs and matrix grains, indicating strong environmental influence on micro-scale morphology. Figure 1E shows the micro-scale morphology of Cu_3Sn grains after 300 min of soldering at 260°C, exhibiting fine equiaxed grains. Zhang et al. (2018) indicated that at the interface between Sn3.0Ag0.5Cu solder and Ni-containing Cu substrate, the IMC layer exhibits scallop-shaped Cu_6Sn_5 and planar Cu_3Sn structures. Figure 1F shows SEM morphology of the SAC305/Cu interface after aging at 150°C for 360 h. With Ni content over 5%, a prismatic $(Cu,Ni)_6Sn_5$ phase forms; IMC grains coarsen further with prolonged aging. Zhao et al. (2019) found that Sn-Cu lead-free solder consists mainly of a β-Sn matrix and Cu_6Sn_5 IMCs; increasing Cu content leads to more abundant and homogeneously distributed Cu_6Sn_5 particles, influencing micro-scale morphology. Yao et al. (2020) demonstrated that Cu_3Sn solder morphology evolves from fine equiaxed grains to coarse columnar grains, forming a mixed structure.

The micro-scale morphology of sintered silver solder has been extensively studied. Long et al. (2021b) demonstrated that adding SiC microparticles enhances density and thermal stability of sintered silver, significantly reducing porosity (Figure 1G illustrates SEM morphology after sintering). K et al. (2023) reported that sintered silver solder composed of 50 nm nanoparticles and 5 μm microparticles exhibits intensified neck growth under high temperatures and shear stress, leading to structural coarsening and reduced porosity (Figures 1H, I). Ma et al. (2017) optimized solder morphology *via* heterogeneous nucleation, using IMCs as nucleating agents to guide tin crystal growth, mitigating performance degradation and improving fatigue and electromigration resistance.

In summary, solder micro-scale morphology is influenced by material composition, processing techniques, and environmental conditions, directly determining macroscopic performance. Understanding microstructural evolution is crucial for improving mechanical stability and reliability of solder joints, reflecting the close relationship between micro-scale morphology and macroscopic performance.

3 Multi-scale mechanics and their numerical approaches

3.1 Microscopic mechanics models based on MD

Molecular Dynamics (MD) is essential for understanding how tiny structures influence material properties. MD simulations use

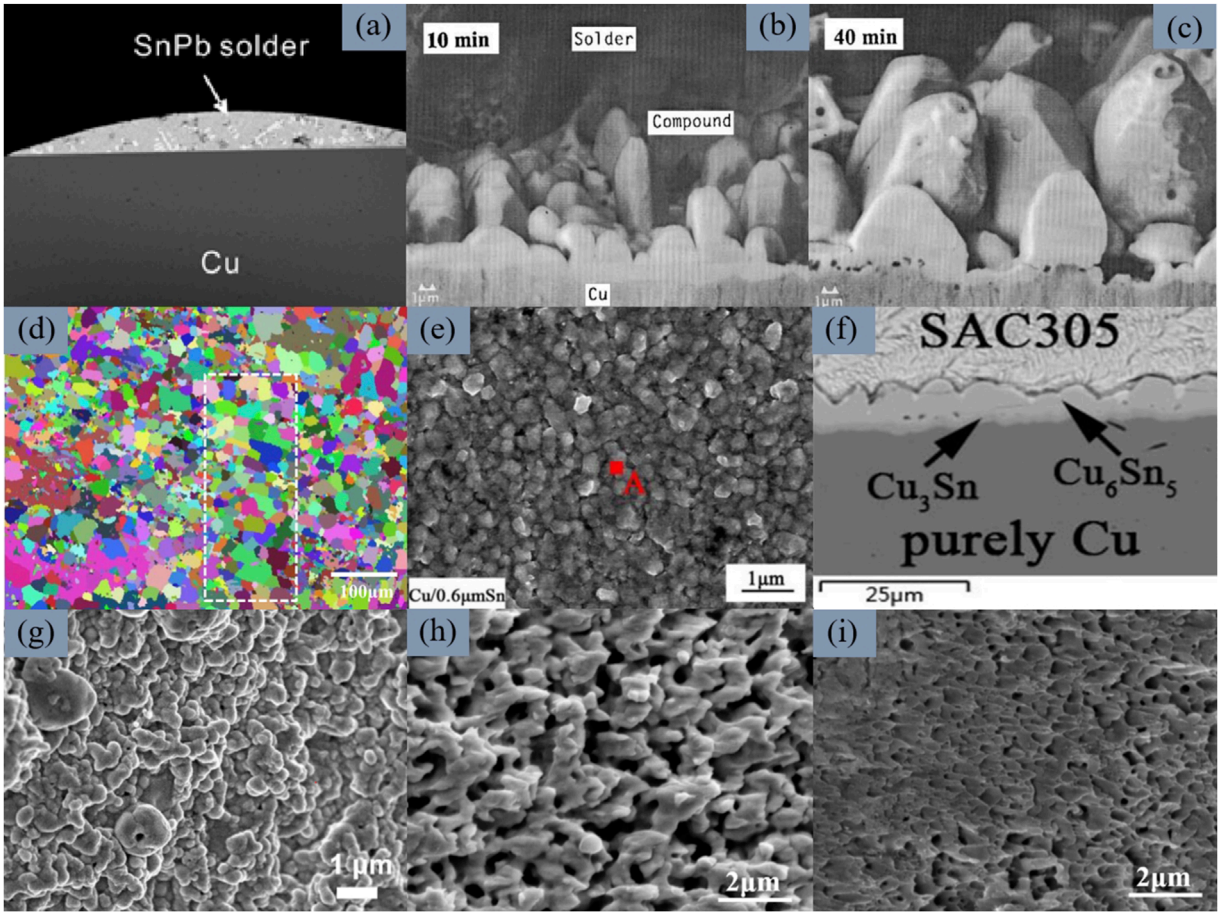

FIGURE 1
Microstructural evolution of different solders. **(A)** Cross-sectional SEM image showing the overall morphology of SnPb solder on copper. **(B, C)** Formation of the Cu_6Sn_5 layer at the SnPb solder interface, which thickens over time and eventually develops into a columnar grain structure. **(D)** Low-magnification EBSD image of as-cast SAC305 alloy, displaying equiaxed Sn grains with diameters of 20–30 μm and varied orientations. **(E)** micro-scale morphology of Cu_3Sn grains after 300 min of soldering at 260°C, showing fine equiaxed grains. **(F)** SEM morphology of the SAC305/Cu interface after aging at 150°C for 360 h **(G)** SEM micro-scale morphology of sintered silver nanoparticles. **(H, I)** SEM micro-scale morphology of the fracture surface of the sintered nanosilver layer at 0°C and 75°C, respectively. [Reprinted from Ref (Tu and Zeng, 2001; Zhang et al., 2007; 2018; Gain and Zhang, 2019; Yao et al., 2020; Long et al., 2021b; Ma et al., 2023). with permission from Elsevier].

techniques like the Embedded Atom Method (EAM) to track atom movements by solving basic physics equations. This helps reveal how small-scale features affect how materials perform. In electronic packaging, MD simulations examine how metal grains interact, how grain boundaries change, and how these factors impact strength and heat resistance. Key materials studied include nanoscale silver, nanoscale copper, SAC305 solder, and intermetallic compounds (IMCs). This knowledge supports improving material performance and enhancing packaging processes.

Haris et al. (2021) reviewed the fundamentals of MD simulations, covering their basic principles, methods, and applications. They used MD simulations to uncover atomic-level details of how molecules interact with metal surfaces. These interactions are difficult to observe using other techniques. Luo et al. (2024) employed MD simulations to investigate sintering processes and mechanical property evolution of copper nanomaterials at 500–650 K. They analyzed microstructural changes of nanospheres and nanofilms under varying sintering conditions, establishing quantitative relationships with shear and tensile properties. These transformations significantly influenced mechanical strength and stability, providing theoretical support for developing high-reliability copper-based packaging materials. Alarifi et al. (2013) utilized MD simulations to analyze sintering and surface premelting behavior of silver nanoparticles, revealing how atomic-scale processes like neck formation and grain boundary evolution affect densification and shrinkage. Gu et al. (2022) investigated atomic motion of silver nanoparticles during sintering, elucidating wetting behavior of smaller particles on larger ones, correlating this behavior with structural rigidity and bonding strength.

Hu et al. (2023) explored sintering mechanisms of silver nanoparticles at different temperatures and their impact on mechanical properties. The study revealed roles of neck growth and dislocation evolution in determining material strength and plastic deformation, providing theoretical support for optimizing silver-based packaging materials. Motalab et al. (2019) investigated influence of micro-scale morphology of SAC solder at nanoscale

on material properties using MD simulations. They found that formation of IMCs like Ag_3Sn enhances strength and modulus while reducing ductility and thermal conductivity. Ye et al. (2024) employed MD simulations to investigate neck evolution mechanisms of silver nanoparticles on SiC/Cu substrates during sintering, revealing how microscopic changes in neck width influence mechanical properties of the sintered interface. Zhang and Liu (2024) analyzed effects of sintering pressure and temperature on mechanical properties of silver nanomaterials under uniaxial tension, revealing how microscopic energy changes, density, and dislocation evolution regulate yield strength and deformation behavior, providing guidance for optimizing sintering processes.

Although MD simulations have advanced our understanding of microstructures and properties in materials like copper, silver, and SAC solder, most studies focus on specific materials, limiting their broad applicability. Additionally, simulations are not well integrated with experiments, making it hard to predict real-world behavior. High computational demands also restrict large-scale use. In the future, research should explore more materials, improve experimental validation, and optimize multiscale simulation methods to enhance the reliability and efficiency of electronic packaging material design.

3.2 Meso-scale models on crystal plasticity and fracturing

Mesoscopic models—including crystal plasticity, cohesive, and phase-field models—capture aspects of the relationship between meso-scale structure and macroscopic performance. Crystal plasticity focuses on crystallographic orientation and slip mechanisms, while phase-field models reveal the influence of phase transformations and crack propagation through meso-scale evolution.

Xie et al. (2021) applied the Crystal Plasticity Finite Element Method (CPFEM) to simulate mesoscopic deformation mechanisms like slip and dislocation motion in SAC305 solder, linking microstructural features like β-Sn dendritic and eutectic regions with macroscopic mechanical response under thermal aging (Xie et al., 2022). Jiang et al. (2024) used phase-field models to simulate the meso-scale structural changes in sintered silver during thermal aging. They incorporated structures with varying porosity into finite element models to show how pore evolution impacts thermal and mechanical properties. This work provides a multiscale framework for evaluating reliability.

Long et al. (2023a) incorporated crystal plasticity models to account for grain orientation and pore distribution on mesoscopic deformation behavior, revealing how pore structures and grain orientation under thermal cycling induce non-uniform stresses and crack propagation. Su et al. (2021b), Su et al. (2023) developed advanced phase-field models that incorporate micro-scale morphology and account for thermo-elasto-plastic coupling. They explained how porosity affects the growth of large-scale cracks. Their models provide reliable predictions of thermal fatigue behavior in sintered silver and other porous materials.

Xie and Chen (2022) integrated thermal activation mechanisms into their crystal plasticity model to investigate cyclic softening and creep behavior under thermomechanical coupling, showing how grain orientation and temperature affect macroscopic properties. Zhu et al. (2021) employed phase-field models to examine fracture behavior of sintered silver nanoparticles with varying porosities, emphasizing the significant impact of mesoscale structure on properties like elastic modulus and ultimate strength. Long et al. (2023b) used a damage-based CPFEM to simulate plastic deformation and damage evolution in nickel-based polycrystalline alloys under low-cycle fatigue, demonstrating how mesoscopic features influence macroscopic mechanical behavior, effectively bridging the gap between mesoscopic and macroscopic responses.

Although crystal plasticity and phase-field models have advanced the simulation of mesoscale behaviors in materials like SAC305 solder and sintered silver, issues remain. These models are computationally complex, limiting large-scale simulations, and often focus on specific materials and conditions, lacking generality. Parameter calibration heavily relies on experimental data, increasing implementation difficulty. Additionally, some studies do not adequately integrate multiscale methods, affecting predictions of actual performance. In the future, computational efficiency should be optimized, the range of applicable materials expanded, and integration with experimental data strengthened to enhance model practicality and accuracy.

3.3 Macroscopic constitutive models and simulation methods

3.3.1 Macroscopic constitutive models

Macroscopic constitutive models are crucial for understanding the mechanical reliability of chip support materials, serving as a cornerstone in multiscale analysis by describing material responses to applied loads and connecting micro- or meso-scale mechanisms to macroscopic performance. They capture elastic, plastic, and creep behaviors, enabling predictions under various conditions.

Significant progress has been made in viscoplastic constitutive models for solder materials. Anand (1982) introduced strain rate and temperature-dependent constitutive equations, initially for high-strength aluminum, later applied to SnPb and lead-free solders. Building on Anand's model, Motalab et al. (2014) derived creep responses for SAC305 solder joints, with fitted parameters aligning with experimental trends. Pei and Qu (2005) refined the linear relationship between Anand model parameters and temperature for lead-free solders, improving data fitting accuracy. Long et al. (2017), Long, et al. (2020) used a modified UCP model for SAC305 deformation at low to moderate strain rates and the Johnson-Cook model for high strain rate impacts. These studies highlight the importance of macroscopic constitutive models in enhancing performance predictions.

In materials science, these models are essential in multiscale analysis frameworks. The Anand model, applied by Calabretta et al. (2021), accurately simulates temperature and strain rate effects on mechanical behavior, especially viscoplasticity. However, it heavily relies on experimental data; recharacterization is necessary for new materials or scenarios. Chen et al. (2014) integrated the Ohno-Wang (OW) model with the Anand model in ABAQUS to simulate shear and creep behavior of sintered nanosilver joints, with experimental validation showing the OW model outperforming Anand's under high-temperature conditions. Gharaibeh and

Wilde, 2023 evaluated several parameter sets for the Anand model. They examined how different creep constitutive models affect simulations and highlighted the importance of multiscale analysis in selecting a model. Lederer et al. (2021) developed a constitutive equation encompassing plasticity, creep behavior, and porosity impact on sintered silver joints, implemented in ABAQUS using UMAT and VUMAT subroutines. Long et al. (2023d) stressed the importance of nanoindentation techniques in investigating elastoplastic properties of sintered silver joints, confirming that combining nanoindentation and numerical methods offers comprehensive nanoscale understanding, aiding design and performance optimization (Long et al., 2024).

Although macroscopic constitutive models have improved our understanding of solder materials' mechanical reliability, they have some limitations. They rely heavily on experimental data, requiring recharacterization for new materials, which is time-consuming. Combining multiple models increases complexity and may reduce accuracy. Many studies do not validate models in different scenarios, limiting their general use. Future research should make models more flexible, simplify integration, and increase validation efforts to enhance their reliability and usefulness in multiscale analyses.

3.3.2 Long-term performance analysis

Long-term performance analysis is vital for predicting material reliability under specific operating conditions, particularly in understanding fatigue and creep behaviors. High temperatures and cyclic loading introduce complex failure mechanisms across micro-, meso-, and macro-scales. Structural characteristics like grain structure, defects, and crack propagation at micro- and meso-scales play pivotal roles.

Chen et al. (2020) demonstrated that sintered silver paste, while exhibiting excellent fatigue resistance at room temperature, deteriorates significantly at 200°C due to increased plastic deformation and accelerated crack propagation (Figure 2A shows SEM image of surface cracks after fatigue testing at 200°C). Zhang et al. (2024) found that meso-scale defects in sintered silver nanoparticles affect macroscopic crack propagation by inducing stress concentration and dislocation emission. Rectangular defects delay failure and enhance toughness by dispersing stress, whereas arc-shaped and triangular defects accelerate crack propagation, leading to faster failure (Figure 2B illustrates the evolution of fatigue cracks in sintered silver chip interconnections simulated by the phase-field method).

Su et al. (2021a) used finite element and phase-field simulations to investigate the impact of power cycling on sintered silver bumps, revealing that cracks initiate from chip corners and propagate toward the center (Figure 2C). Thermal performance decline becomes more pronounced during long-term degradation (Chen et al., 2022). For SAC305 solder, a novel fatigue damage model based on entropy increase showed a strong correlation between damage parameter evolution and strain rate, providing theoretical support for predicting long-term performance of electronic packaging structures (Long et al., 2023f).

At the macro-scale, cumulative effects of micro- and meso-scale mechanisms manifest as global material failure, such as changes in crack propagation and fracture modes. Multiscale analysis effectively links the evolution of micro-scale morphology and meso-scale structures to macroscopic mechanical performance, providing a reliable foundation for describing material failure under high-temperature conditions. This approach is valuable in electronic packaging and high-temperature applications, offering robust support for design optimization and long-term performance prediction (Long et al., 2021a). Su et al. (2022) further verified the importance of multiscale analysis in failure prediction by analyzing the impact of thermal cycling loads, power density, and switching frequency on crack propagation rate and morphology using a fracture phase-field model.

A study using a thermo-elasto-plastic phase-field model investigated how randomly distributed micro-scale morphology influences the long-term performance of sintered nano-silver materials, focusing on the role of meso-scale pore evolution in crack propagation and network formation (Agyakwa et al., 2020; Su et al., 2021b). Additionally, a new Unified Creep Plasticity (UCP) constitutive model reveals the accumulation and evolution of fatigue damage in viscoplastic materials under varying temperatures and strain rates, offering theoretical insights for material design optimization and reliability enhancement (Long et al., 2023e). Figure 2D shows crack propagation in sintered nano-silver under thermo-elasto-plastic phase-field modeling, comparing experimental results and numerical simulations.

While multiscale analysis effectively connects micro- and meso-scale phenomena to macroscopic performance, it has limitations. The models are often computationally intensive, making large-scale simulations challenging. Additionally, many studies focus on specific materials like sintered silver and SAC305, reducing their general applicability. Experimental validation is sometimes insufficient, which can undermine the reliability of predictions. Future research should aim to streamline models, expand the range of studied materials, and enhance experimental correlations to improve the accuracy and applicability of long-term performance predictions in electronic packaging.

4 Next steps and perspectives

As electronic packaging interconnect materials evolve toward miniaturization, high integration, and multifunctionality, multiscale approaches have become increasingly important. Multiscale modeling will play a crucial role in optimizing design and assessing reliability of packaging materials. By integrating methods like Crystal Plasticity Finite Element Analysis, phase-field modeling, and MD simulations, researchers can more accurately uncover mechanisms driving material evolution. Structural features like grain size, pore distribution, and interfacial properties can be incorporated into macroscopic models, enhancing performance prediction accuracy. These approaches are expected to find broad applications in advanced solder materials, nanomaterials, and heterogeneous packaging systems to meet complex demands of modern packaging.

Advancements in multiscale methods will facilitate a shift in material design from experience-based to theory-driven approaches. Implementing Artificial Intelligence (AI) and Machine Learning (ML) can accelerate extraction and validation of parameters across scales, simplifying simulations and enhancing computational efficiency. This transformation shifts from traditional experimental approaches to systematic, computer-aided

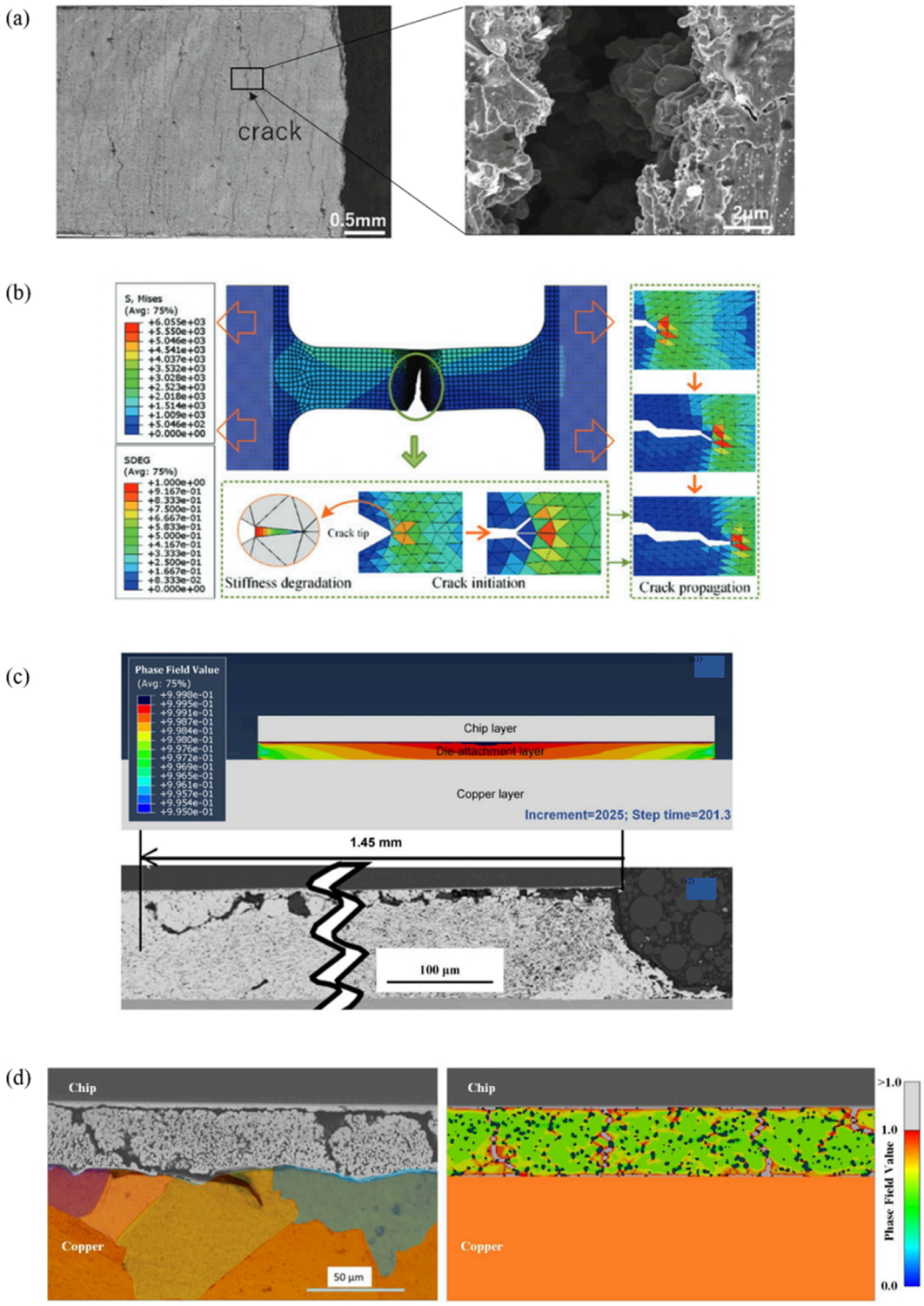

FIGURE 2
Fatigue Crack Evolution and Macroscopic Crack Growth in Sintered Silver: Phase-Field Simulation and Experimental Analysis. **(A)** SEM image of surface cracks in a sintered silver specimen after fatigue testing at 200°C. **(B)** Fatigue crack evolution in sintered silver die-attachment based on phase-field simulation. **(C)** Macroscopic crack growth in sintered AgNPs specimens. **(D)** Crack propagation in sintered nano-silver under thermo-elasto-plastic phase-field modeling: comparison between experimental results and numerical simulation. [Reprinted from Ref (Chen et al., 2020; Su et al., 2021b; Su et al., 2021a; Zhang et al., 2024). with permission from Elsevier].

performance optimization, improving scientific rigor and efficiency. However, integrating experimental validation with multiscale modeling remains a critical research focus. Experimental data will continue to calibrate and validate models, improving accuracy and reliability, providing deeper insights into how micro-scale and meso-scale mechanisms influence macroscopic performance. In summary, multiscale analysis will continue to play a pivotal role in packaging material research, driving development of high-performance materials and offering theoretical support for high-density, highly reliable electronic products.

5 Conclusion

This review systematically examines advancements in cross-scale modeling of interconnect materials used in electronic packaging, analyzing intrinsic correlations between micro-scale and meso-scale structural features and macroscopic mechanical properties. Conventional macroscopic constitutive models have limitations in capturing mechanical behavior of complex packaging materials, making it challenging to reflect influence of structural evolution on overall performance and failure mechanisms. Through multiscale simulation techniques like MD, CPFEM, and phase-field models, researchers can precisely reveal mechanical responses across scales and conduct in-depth analyses of failure mechanisms in solder and sintered material systems. This paper summarizes strengths of these approaches in describing evolution of defects, grain orientation changes, and pore distribution, exploring potential applications under complex stress conditions.

Cross-scale modeling connects micro- and meso-scale mechanisms with macroscopic performance, enhancing material reliability and design accuracy, especially in long-term performance analysis. This review highlights the profound impact of micro-scale morphology and meso-scale structure on mechanical properties, providing theoretical support for optimizing electronic packaging materials design.

Author contributions

ZeZ: Investigation, Methodology, Visualization, Writing–original draft. FL: Methodology, Writing–review and editing. VF: Methodology, Writing–review and editing. ZoZ: Conceptualization, Supervision, Writing–original draft, Writing–review and editing. SL: Funding acquisition, Methodology, Supervision, Writing–review and editing. RD: Methodology, Writing–review and editing.

Funding

The author(s) declare that financial support was received for the research, authorship, and/or publication of this article. This work was supported by the National Natural Science Foundation of China (Nos. 52475166, 52175148), the Regional Collaboration Project of Shanxi Province (No. 2022104041101122), the Qin Chuang Yuan high-level innovation and entrepreneurship talent project (No. QCYRCXM-2022-306), and the Natural Science Foundation of Chongqing (No. CSTB2022NSCQ-MSX0574).

Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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The author(s) declare that no Generative AI was used in the creation of this manuscript.

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frontiers | Frontiers in Electronics

TYPE Review
PUBLISHED 03 February 2025
DOI 10.3389/felec.2024.1515860

OPEN ACCESS

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RECEIVED 23 October 2024
ACCEPTED 30 December 2024
PUBLISHED 03 February 2025

CITATION
Praful P and Bailey C (2025) Warpage in wafer-level packaging: a review of causes, modelling, and mitigation strategies.
Front. Electron. 5:1515860.
doi: 10.3389/felec.2024.1515860

Warpage in wafer-level packaging: a review of causes, modelling, and mitigation strategies

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Wafer-level packaging (WLP) is a pivotal semiconductor packaging technology that enables heterogeneously integrated advanced semiconductor packages with high-density electrical interconnections through its efficient and highly reliable manufacturing processes. Within this domain, fan-out wafer-level packaging has gained prominence due to its potential for high integration capacity, scalability, and performance on a smaller footprint. This review examines FOWLP technology and its associated challenges, primarily warpage. As semiconductor companies strive to develop cutting-edge packages, wafer warpage remains an intrinsic and persistent issue affecting yield and reliability at both the wafer and package levels. Warpage characterization techniques and modeling approaches, including theoretical, numerical, and emerging artificial intelligence and machine learning (AI/ML) methods, have been analyzed. The structural parameters and properties of the constituent materials of the reconstituted wafer and the FOWLP process have been considered to evaluate the effectiveness of these methods in predicting and analyzing warpage. Potential directions and limitations in warpage prediction and mitigation have been outlined for future research for more reliable and high-performance FOWLP solutions.

KEYWORDS

FOWLP, warpage, modelling, advanced semiconductor packaging, heterogeneous integration

1 Introduction

1.1 Advanced semiconductor packaging and heterogeneous integration

In 2015, the International Technology Roadmap for Semiconductors (ITRS), which had served as the premier guide for the semiconductor industry for enabling transistor scaling and progressing Moore's law for the past 22 years, acknowledged the end of Moore's law of transistor scaling, signaling a pivotal shift in the semiconductor industry. The report introduced the concepts of "More than Moore" (MtM) for functional diversification improvements and increasing functional density through heterogeneous integration of diverse digital and non-digtal components at the semiconductor package level (Gargini, 2015). A semiconductor package is a protective casing that contains one or more discrete semiconductor devices or integrated circuits (ICs), providing a means to connect internal components to external circuitry and thermal management structures, and protect them

from contamination. In 2019, the first version of the heterogeneous integration roadmap was published with a strong focus on integration, packaging, testing, and interconnect technology required to meet the needs of advanced technologies such as AI and high-performance computing (HPC) (Chen and Bottoms, 2019).

The semiconductor manufacturing ecosystem comprises two main phases: front-end and back-end. The front-end phase focuses on the fabrication of integrated circuits on semiconductor substrates, while the back-end phase encompasses the testing, packaging, and electrical connectivity of these IC substrates.

Established manufacturing processes and their cost-effectiveness have contributed to the widespread adoption of traditional leadframe and substrate packages, such as Dual-in-Line (DIP), Ball Grid Array (BGA), and Quad Flat No-Leads (QFN) packages, to name a few. Outsourced Semiconductor Assembly and Test (OSAT) companies at the back-end-of-line (BEOL) have handled packaging for decades, primarily optimizing for labor costs and manufacturing simplicity without fully considering the potential for technological advancements. However, as ICs have grown increasingly complex and transistor scaling has approached its physical limits, heterogeneous integration and advanced packaging has emerged as a solution. The demand for compact, high-performance, and cost-effective electronic devices in the consumer electronics market over the past decade has been primarily addressed through System-on-Chip technology. System-on-chip (SoC) is an integrated circuit design that combines numerous or all the high-level functional components of an electronic device onto a single chip, rather than the traditional method of employing separate components mounted on a motherboard or printed circuit board (PCB). However, these monolithic structures can no longer meet the physical and cost demands of emerging applications. As a result, heterogeneous integration (HI) and advanced packaging have become indispensable in addressing the need for high-density system integration by utilizing the System-in-Package (SiP) approach, wherein multiple chips with diverse functionalities are contained within a single package. Figure 1 illustrates an example of advanced packaging, where multiple dies are integrated onto a substrate and mounted on a PCB.

Advanced packaging technologies enable HI by allowing the integration of various chips from different manufacturing technologies, wafers, or even foundries into a single package, offering improved performance, power efficiency, and functionality with new technologies such as 2.5D and 3D integration (Wesling, 2020; Chen and Bottoms, 2017). 2.5D and 3D refer to different levels of integration and stacking of chips within the same package. Typically, chips are packaged individually and mounted on a printed circuit board (PCB). In 2.5D packages, chips are placed side-by-side on an interposer or substrate. Substrates can be made of organic or ceramic materials, whereas interposers are made of silicon, enabling high-density interconnections between the chips. These silicon interposers are produced using chip fabrication processes. In 3D advanced packages, multiple chips are vertically stacked and connected with through-silicon vias (TSVs). TSVs offer high bandwidth and low latency for applications such as high-performance computing and artificial intelligence. Figure 2 illustrates examples of 2.5D and 3D packaging architectures.

The key end applications driving the adoption of advanced packaging technologies are:

1. Autonomous driving
2. Artificial intelligence
3. Consumer electronics
4. Communication and networking infrastrucure
5. High-performance computing
6. Internet of Things (McKinsey & Company, 2025)

Top semiconductor foundries like TSMC, Samsung, and Intel, as well as OSATs such as ASE and Amkor, seek to expand their presence in the advanced semiconductor packaging market as the technology becomes increasingly complex and profitable.

1.2 Wafer-level packaging

Wafer-level packaging (WLP) is a prominent advanced semiconductor packaging technique in which integrated circuits and other components are packaged while still on the wafer. This approach significantly reduces manufacturing costs and improves yields by performing packaging operations on entire wafers. WLP enables the creation of smaller package sizes with enhanced electrical performance, addressing the demand for more compact and efficient electronic devices (Liu et al., 2014). Its scalability and integration capabilities support advanced system-in-package systems and improve package reliability through improved process control (Liu et al., 2014). Furthermore, WLP's compatibility with existing semiconductor manufacturing processes eases its implementation in current facilities. With WLP, wafer-based processing, and front-end fabrication equipment such as using lithography tools can be adapted for creating redistribution layers (RDL). WLP also streamlines back-end processes by reducing assembly steps and enabling efficient wafer-level testing. WLP is an attractive option for various semiconductor applications, particularly in industries where size, performance, and cost are critical factors (Lau, 2018).

1.3 Fan-out wafer-level packaging

One of the latest advances in wafer-level packaging is fan-out wafer-level packaging technology (FOWLP). This approach involves placing dies from different wafers onto a reconstituted wafer and redistributing the interconnects on the wafer, enabling a greater number of input/output connections compared to traditional chip-scale packaging. Fan-out wafer-level packaging also offers other benefits, such as reduced form factor and the ability to integrate multiple passive and active components within a single package. Figure 3 highlights the key differences between traditional packaging, wafer-level packaging, and fan-out wafer-level packaging. In traditional packaging, dies are diced from a silicon wafer and then packaged individually. In contrast, wafer-level packaging involves packaging the dies while they remain on the wafer. FOWLP places the dies onto a temporary carrier wafer, performs molding and other packaging processes, and then proceeds with package singulation.

Furthermore, FOWLP technology can be used in Multi-Chip-Module (MCM) packages that simply integrate chips of different types

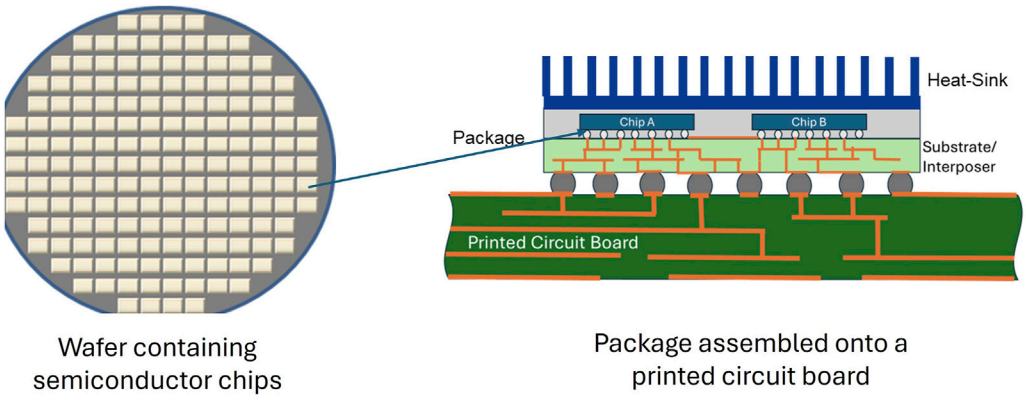

FIGURE 1
Dies integrated within an advanced semiconductor package.

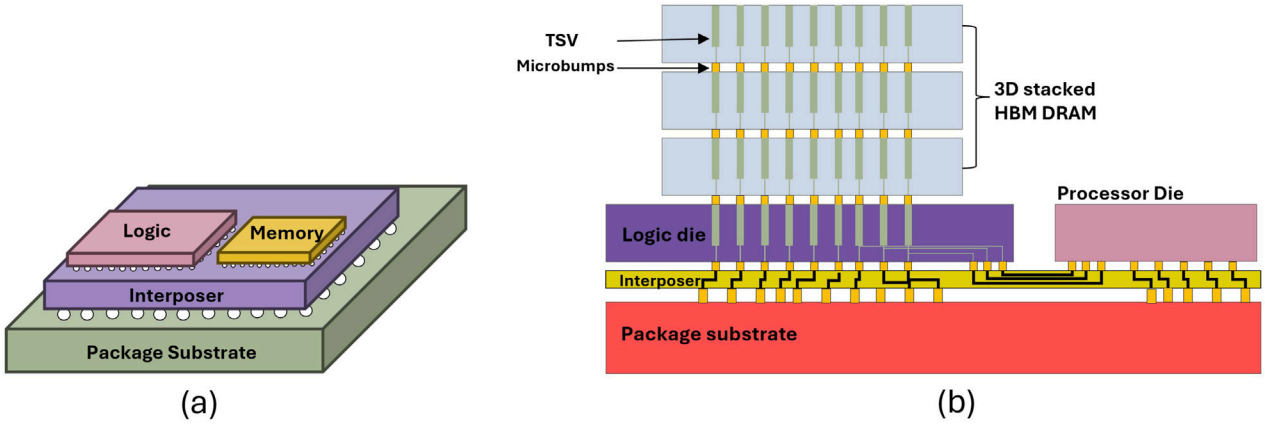

FIGURE 2
(A) 2.5D semiconductor package strucutre **(B)** 3D integration of memory, logic and processor dies within a package.

and sizes into a module or subsystem, or in System-in-Package (SiP) applications that combine diverse chips into a single system. For mid-to high-end device integration requirements in consumer and high-performance computing (HPC) applications, which might typically require an expensive 2.5D interposer with through-silicon vias (TSV), fan-out technology offers a cost-effective alternative (Lim and Wee, 2018). 3D fan-out Package-on-Package (PoP) solutions utilize electrical routing through redistribution layers (RDL) on both the top and bottom faces of packages (see Figure 4) (Sandstrom et al., 2021). Combined with through-mold or through-package vias for communication between packages in the 3D stack, the PoP strucutre enables thinner profiles and smaller footprints on a printed circuit board (PCB). These through mold-vias can also be used for thermal management (Lau and Yue, 2009).

The other type of wafer-level packaging is the fan-in wafer-level packaging or wafer-level chip-scale packaging (WLCSP), typically used for low-end mobile devices with basic technological requirements and lower I/O requirements, and the redistribution layers are routed toward the center of the die. In contrast, fan-out wafer-level packaging features RDLs and solder balls that exceed the size of the die, allowing the chip to have more input/output connections while maintaining a thin profile.

A key driver for fan-out technology has been the need for higher I/O densities and finer RDL with line-space (L/S) measurements ('line' refers to the width of the metal trace, while 'space' refers to the gap between adjacent traces). Fan-out packaging is further divided into three subtypes based on I/O densities and L/S: core, high density, and ultra-high density.

1. Core fan-out packaging with <6 I/O per mm^2 and RDL L/S $>15\mu$m/15μm is used primarily for automotive and network applications.
2. High density fan-out packaging with $6<$ I/O per mm^2 <12 and 15μm/15μm $<$ RDL L/S $>15\mu$m/15μm are predominantly used for mobile applications and Antenna-in-Package (AiP).
3. Ultra high density (UHD) FO packaging with $\gg 18$ I/O per mm^2 and RDL L/S $\ll 5\mu$m/5μm are used for network and server applications.

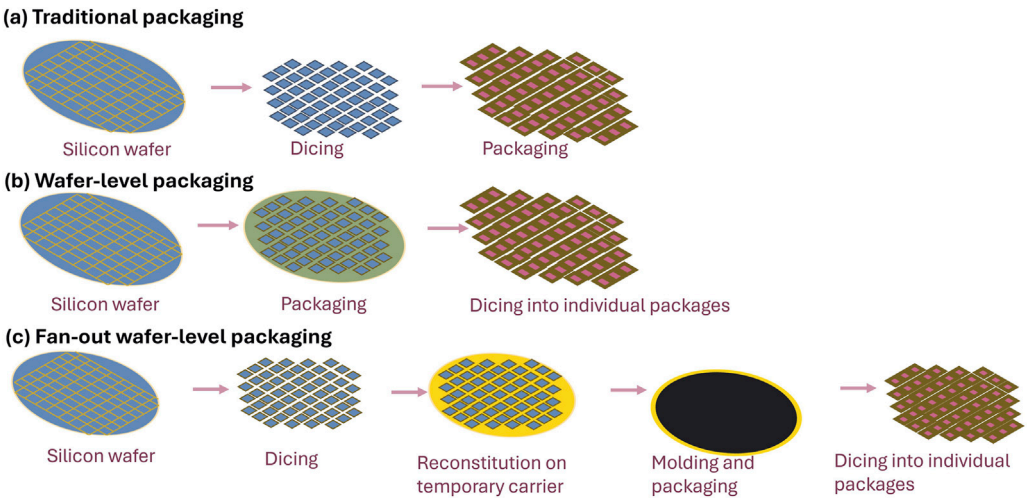

FIGURE 3
(A) Traditional packaging process **(B)** Wafer-level packaging process **(C)** Fan-out wafer-level packaging process.

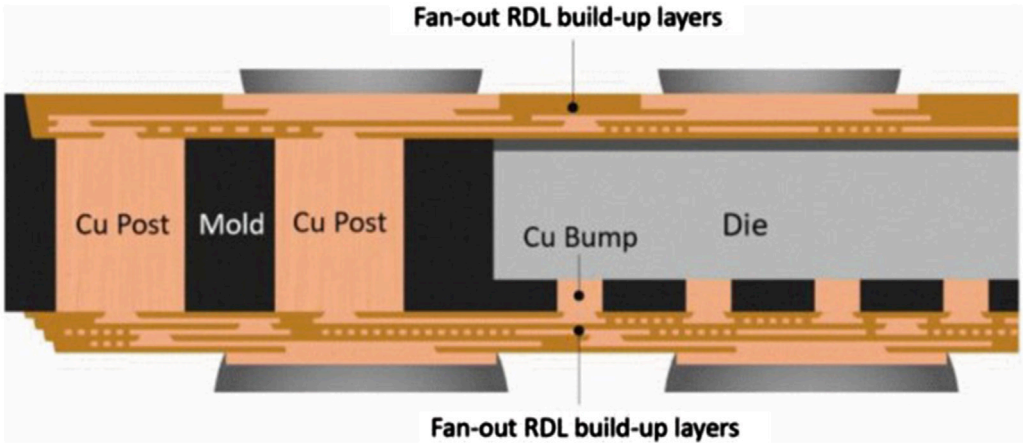

FIGURE 4
Fan-out RDL layers on top and bottom faces of a Deca M-Series™ 3D PoP (Sandstrom et al., 2021). Reprinted with permission from IEEE Proceedings.

Fan-out technology was first developed at Infineon between 2001 and 2007 with the creation of the embedded wafer-level BGA (eWLB). The eWLB was subsequently licensed by Infineon to other Outsourced Semiconductor Assembly and Test (OSAT) companies, including ASE, Amkor Portugal, JCET Group, and STMicroelectronics, for manufacturing their own line of products. In 2016, wafer-level fan-out packaging gained significant attention when Taiwan Semiconductor Manufacturing Company (TSMC) announced the use of their fan-out (FO) product, Integrated Fan-Out (InFO), to package the application processor engines (APE) for Apple's iPhone 7. Since then, Apple has become the largest original equipment manufacturer (OEM) to be the largest consumer of FO technology. TSMC is the largest supplier of FO in the world and has continued to expand its FOWLP offerings, developing derivatives such as InFO AiP (Antenna in Package) and InFO PoP (Package in Package) to cater to the networking and high-performance markets (Keser and Kröhnert, 2019).

Future development in FOWLP is to fabricate more RDL layers on the wafer to accommodate greater I/O, which necessitates finer line/spacing $<2\mu$m (Davis, 2022). The manufacturing issues that need to be overcome are die shift and wafer warpage during the manufacturing processes. DECA technologies has addressed die shift through its adaptive patterning technology, which provides an EDA (Electronic Design Automation) methodology to design during manufacturing (DDM), where die shift is accommodated through rerouting of the conductive tracks to ensure connections are made between components (Bishop et al., 2016).

Deca developed the unique M series FOWLP in 2012 that employs their proprietary Adaptive Patterning™, enabling high-density integration and improved yields for multichip modules (Bishop et al., 2016). The Deca M-series features a fully encapsulated structure and a proprietary planarized surface with a molded stress buffer layer over the active device surface. The M-Series offers multiple variants such as multi-die packaging,

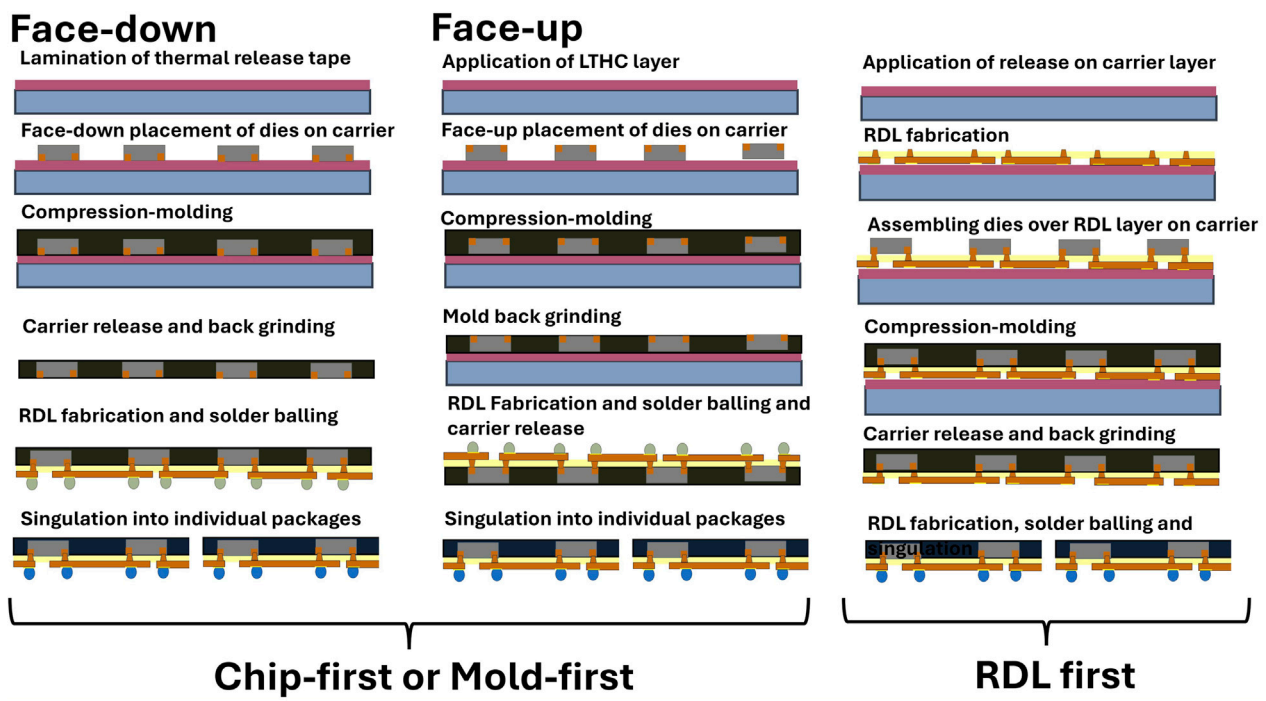

FIGURE 5
Fan-out packaging approaches.

chiplet integration, 3D PoP, and embedded bridge die interposers. With 3D configuration capabilities, embedded components, and fine-pitch connections on both sides of an organic interposer, the M-Series has been adpated for high-performance applications such as AI and HPC.

2 Fan-out wafer-level packaging process flow

2.1 FOWLP packaging approaches

Classical wafer-level packaging process begins with wafer preparation, including back grinding and dicing operations. Redistribution layers are created through dielectric application and copper plating. Photolithography, sputtering, and electroplating are used to form the desired patterns and metal layers. After photoresist stripping and metal etching, a dielectric layer is applied as a protective coating. Solder balls are then attached, followed by electrical testing and final wafer dicing. FOWLP distinguishes itself from conventional wafer-level packaging with the reconstitution process, where the fan-out region is developed over a molded wafer (also called a reconstituted wafer). Different fan-out approaches, such as chip-first die face-down and die face-up, and chip-last or RDL-first as shown in Figure 5, have evolved to address diverse application requirements and overcome manufacturing limitations (Lau, 2022).

1. Chip-first die face-down: Known good dies (KGDs), singulated from the device wafer, are attached face-down to a temporary wafer with a thermal release tape. After compression molding with liquid EMC to encapsulate the silicon die and post-mold cure (PMC), the temporary wafer is removed with a thermal debonding step. Redistribution layers (RDLs) for electrical signal routing are built on the backside of the exposed dies. Solder balls are then mounted over designated spots on the RDL layer to establish connection between the chip package and an external printed circuit boards (PCB) before reconstitued wafer is singulated into individual package entites.
2. Chip-first die face-up: On the origial device wafer, copper studs are prefabricated using electroplating. These dies are then assembled using a high-speed pick-and-place tool on a reconstituted wafer. The wafer is then molded with compression molding and cured. The EMC at the top of the wafer is backgrinded to expose the copper studs, and RDL layers are developed.
3. Chip last or RDL first: RDL layers are first fabricated on the reconstituted wafer. The KGDs of the original device wafers are then placed on top of the reconstituted wafer with RDL. Compression molding is performed next, followed by backgrinding and debonding from the temporary wafer carrier. Solder balls are mounted and the wafer is singulated into individual packages.

Although wafer-level packaging has an established infrastructure, the industry is also transitioning to panel-level packaging primarily due to cost reduction and increased productivity. Panel-level packaging can reduce costs by more than 20%, especially for larger package sizes, by using rectangular panels that offer more space. This approach achieves up to 95% area usage compared to 85 for round wafers, allowing for more packages per carrier and reduced handling time. Adopting panel-level fan-out

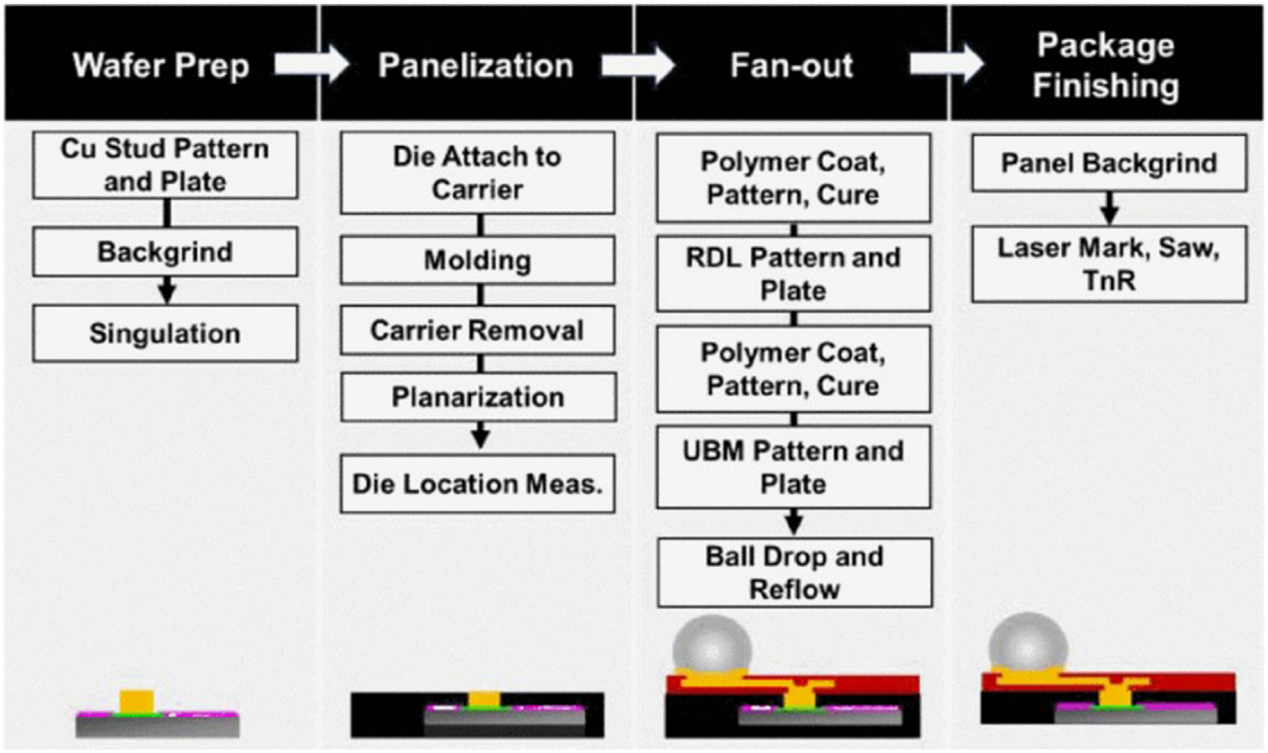

FIGURE 6
Deca's M-series chip-first process flow for a fully molded FOWLP. Reprinted with permission from IEEE Proceedings (Sandstrom et al., 2021).

packaging could enable higher throughput, better area utilization, lower costs, and scalability (Braun et al., 2019; Lau et al., 2020; Braun et al., 2021; Braun et al., 2018).

2.2 Warpage evolution in FOWLP process flow

The fan-out wafer-level packaging process involves multiple temperature excursions and pressure conditions, which can induce different stress states and lead to warpage at the wafer and package levels (Lau et al., 2018a; Lau al., 2018b). Fundamentally, warpage is an out-of-plane deformation. The FOWLP manufacturing line must follow a rigorous sequential process to maintain uninterrupted production and maximize yield. Warpage can disrupt the manufacturing process, making it difficult for various equipment to handle deformed wafers. Wafers with coplanarity issues may also face misalignment during RDL build-up, ball placement, and wafer singulation processes, leading to degradation in the reliability of the final packages or even delamination and breakage of the wafer (Chen et al., 2022).

Deca's M-Series employs a unique chip-first face-up approach to FOWLP that has drawn considerable attention in the industry due to its high yield and reliability (Shoo et al., 2019). To understand the evolution of warpage in one of the latest FOWLP manufacturing processes, the Deca M series process can be examined as an exemplary as shown in Figure 6 (Rogers et al., 2017).

1. Wafer prepararion: This step includes the fabrication of copper studs on the device wafer. The seed layers are sputtered and a thick photoresist is patterned. Copper studs are electroplated over the under bump metallization (UBM), stripping and etching the photresist and seed layers. The top of the device wafer is coated with a polymer, and its bottom side is laminated with a die-attach film (DAF). The wafer is singulated into individual chips.
2. EMC Molding and Curing: The dies are aligned with their active side face-up precisely on a reusable temporary carrier at designated fan-out pitches. EMC is dispensed over the reconstituted carrier wafer and compression molding is performed in a mold cavity to encapsulate all components on the carrier under timed pressure and temperature conditions. After the initial molding process (in-mold cure or IMC) to solidify the viscous EMC, a post-mold cure (PMC) step at temperatures higher than those of IMC is required to complete the curing and stabilize the EMC. The cured carrier is then cooled to room temperature.

The first significant warpage occurs after the post-mold cure process. This warpage is primarily attributed to the mismatch in coefficient of thermal expansion within the die-mold-carrier

assembly stack, as well as the evolving properties of the encapsulating EMC (Lau, 2018).

This carrier is detached from the carrier from the reconstituted wafer through a debonding step. The warpage of the reconstituted wafer is significantly increased during the debonding process, as the stresses accumulated in the wafer are suddenly released and redistributed (Lin et al., 2016; Lim et al., 2018). EMC molding is removed using a backgrinding machine to reveal the Cu contact pads over which RDL layers will be developed. The backgrinding process can induce mechanical stresses that impact wafer warpage.

Optical scanning is later used to record the location of every die on the reconstituted wafer.

3. RDL fabrication: This stage includes curing and patterning of dielectric polymer to provide insulation between copper traces in the RDL layer. The Cu RDL layers are then patterned and electroplated over the exposed Cu studs' surfaces to reroute the die's input/output (I/O) connections from their original locations to new positions in the package area.

The differences in Young's modulus and coefficient of thermal expansion between the photosensitive polyimide and copper traces create an uneven stress distribution across the assembly, leading to warpage.

Flux is applied to the solder ball attachment areas, and the solder balls are then mounted through the solder reflow process. The peak temperature reached during this reflow step is 200°.

The reflow process introduces thermal stress due to temperature changes, aggravating warpage from CTE mismatches. Additionally, the mounting process itself can introduce new stresses and deformations, potentially altering the package's post-manufacturing warpage characteristics.

4. Package finishing: In the last step, backgrinding is performed to thin the package and the packages are singulated.

Warpage, die-shift and RDL processing are closely interrelated. Warpage in the reconstituted wafer can directly cause die shift, as the distorted wafer surface may disrupt the alignment of dies placed on the carrier. Excessive warpage also hinders lithography tools from correctly patterning RDL traces on the wafer or panel. RDL fabrication relies on high-precision photolithography to pattern fine interconnects between chips. If the wafer has warped or the dies have shifted, the RDL layers may not align correctly with the underlying dies, leading to faulty or incomplete connections. Warpage can also cause variation in layer thickness, which impacts electrical performance and increases the risk of shorts or open circuits. Thus, improved warpage management and die shift control can ease the RDL patterning process. To achieve these goals, process control plays a critical role across all areas of semiconductor manufacturing, enabling high yields and better profit margins (Lu, 2018).

3 Measuring warpage

The Semiconductor Equipment and Materials International (SEMI) organization characterizes the warpage of wafers with respect to the orientation of its functional surface. When viewed from the functional surface as depicted in Figure 7, if the center is depressed and the edges protrude upward concavely, this constitutes a positive warpage value (smiling face). In contrast, a negative value (crying face) is indicated by a convex shape with the center protruding and the edges depressed downwards.

Temperature-dependent warpage can be measured with non-contact moiré-based methods such as thermal shadow moiré and digital fringe projection (DFP). Digital image correlation (DIC) is a non-contact, stereo-vision based method that can capture dynamic warpage behaviour. While there are several moiré-based techniques available, including shadow moiré, laser fringe projection, and digital fringe projection, and other non-contact techniques this discussion will focus specifically on shadow moiré, DFP, and DIC as these methods seem to be the most widely adopted metrology tools for wafer warpage (Sun and Zhang, 2024).

3.1 Moiré-based measurement

Moiré-based optical methods measure surface deformations and displacements by analyzing interference patterns, called moiré fringes, created by the superimposition of two similar patterns.

Shadow Moiré is a relatively simple optical technique used to measure out-of-plane deformations and surface profiles by analyzing moiré fringes generated by a diffused light source and a reference grating. A CCD (Charge-Coupled Device) camera, captures images of these fringes (see Figure 8), which are then processed to reconstruct the out-of-plane topography of the surface, as shown in Figure 9. The sensitivity and resolution of the measurement are primarily controlled by the pitch (line spacing) of the reference grating, with finer gratings generally providing higher sensitivity. Shadow Moiré offers advantages such as full-field measurement capability, dynamic real-time display of deformations, and a simpler setup compared to other optical measurement methods (Sun and Zhang, 2024).

Digital fringe projection involves projecting fringes at an angle onto a sample, as shown in Figure 8, which are then captured by a camera. The system also records the phase information of the fringes at each point as the sample's surface topography changes. DFP leverages these phase data to generate high-resolution 3D representations of a wide range of surfaces, enabling the measurement of both in-plane and out-of-plane deformations. However, DFP tools require a calibration process that could potentially affect the quality of sample measurement (Hubble and Weaver, 2017).

Both shadow moiré and DFP have quick data acquisition capabilities, provide sub-mil or more resolution, and heating chambers with fast temperature ramping for dynamic warpage measurement; shadow moiré provides only single-sided heating that can lead to non-uniform heating of the sample, whereas DFP can uniformly heat both sides (Hubble and Weaver, 2017).

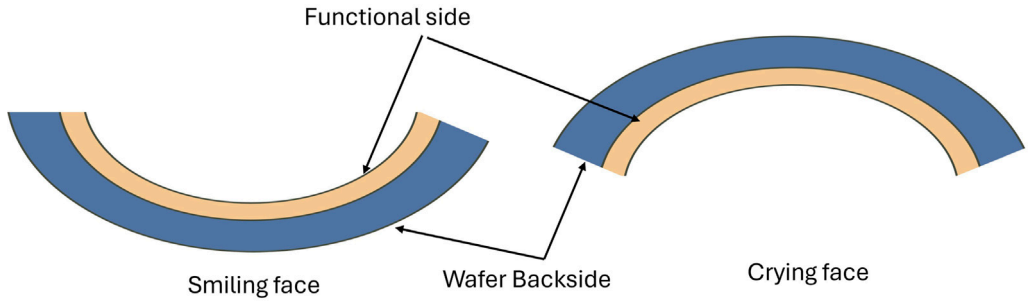

FIGURE 7
Definition of warpage orientation.

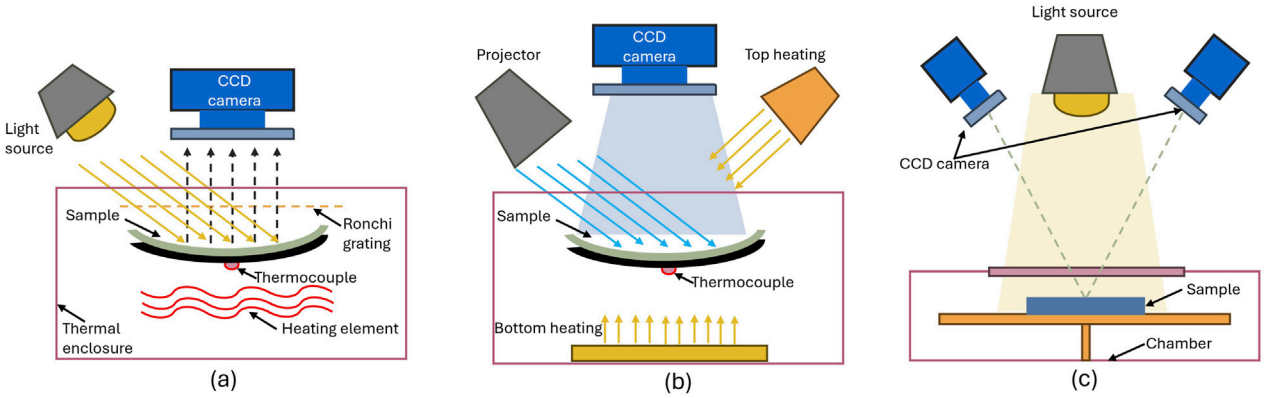

FIGURE 8
(A) Shadow Moiré setup **(B)** Digital fringe projection Setup Set **(C)** DIC setup.

3.2 Digital image correlation

Digital image correlation (DIC) is a stereo vision-based optical technique used to measure full-field displacements and strains on material surfaces by tracking the movement of a random speckle pattern applied to the specimen as the material deforms. A basic DIC setup includes one camera for 2D measurements or two cameras for 3D measurements, lenses, lighting, a speckle pattern on the specimen surface, and DIC software for image processing and analysis (see Figure 8) (Sutton and Hild, 2015).

DIC measurements require speckle patterns that display high contrast, random features, proper deformation with the specimen surface, and appropriate sizing for the field of view and resolution. These speckle patterns are typically applied using techniques such as spray paint, airbrush, stencils, or toner powder, and the quality of their application affects measurement accuracy. Advanced image processing algorithms track the deformation of the speckle pattern between images with subpixel accuracy, allowing DIC to achieve high measurement precision (Sun and Zhang, 2024).

While extensive sample preparation and reliance on computer algorithms for good measurement results present challenges, DIC offers unique advantages such as high-throughput measurement of coefficient of thermal expansion (CTE) and real-time, *in-situ* measurements during processes like solder reflow for packages. Additionally, DIC experimental data can be linked with CAD tools and finite element analysis (FEA) simulations. Loading histories and boundary conditions of DIC experiments can be monitored and applied to FEA software for simulation accuracy. DIC experimental results can be compared to FEA predictions in CAD environments (Sutton and Hild, 2015).

While shadow moire, DFP and DIC are noncontact full-field metrology tools for warpage, the choice for a particular experiment depends on specific requirements such as the need for *in situ* measurements, surface characteristics of the wafer, and the type of deformation (out-of-plane only or both in-plane and out-of-plane).

3.3 Critical warpage thresholds and their impact on manufacturing yield

The warpage thresholds for a 300 mm reconstituted wafer is 1 mm, beyond which handling and subsequent process

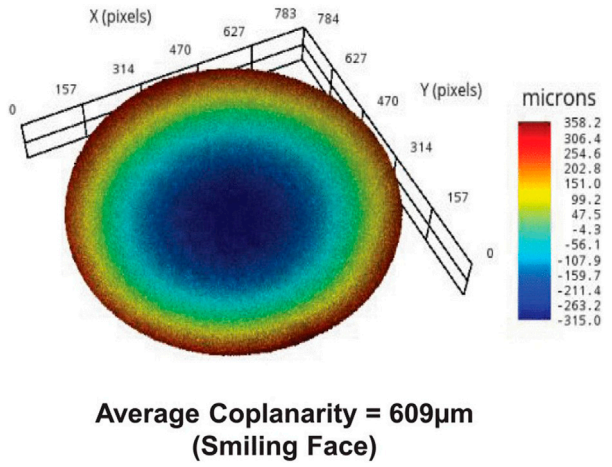

FIGURE 9
Shadow moiré warpage measurement of reconstituted wafer. Reprinted with permission from IEEE Transactions on Components, Packaging and Manufacturing Technology (Lau et al. 2018b).

integration become challenging, affecting the manufacturability and reliability of the final devices. For high yields, warpage should be less than 0.5 mm (Lau, 2019b). The maximum allowable warpage of an individual package is recommended to be 0.2 mm, but 0.1 mm is preferred for high yield (Lau et al., 2018b).

4 Modelling warpage

Experimental, analytical, and numerical methods are essential to predict and control warpage in wafer-/panel-level fan-out manufacturing, considering the complex interplay of constituent material properties, structural and geometric parameters, and process dependencies.

4.1 Material data for warpage analysis and modelling

Warpage modeling approaches are intrinsically dependent on extensive material characterization to ensure accuracy and reliability in their results. Compression molding is one of the initial stages where considerable warpage is observed, and this warpage is attributed to the temperature and cure-dependent behavior of the EMC. As a result, characterizing the material properties of the EMC is a key step in warpage analysis, and assuming simple elastic properties for the EMC can overestimate warpage, as demonstrated in Figure 10.

4.1.1 EMC material properties

1. Estimation of chemical shrinkage and coefficient of thermal expansion of EMC: The EMC is a composite material with epoxy resin as a matrix and silica particles as a filler. As the temperature increases during mold curing and post-curing processes (typically 130°C–175°C), the polymers in the EMC cross-link and solidify, causing a volumetric shrinkage known as chemical shrinkage (Phansalkar et al., 2022). As the EMC cures, it contracts, causing volume reduction and generating internal stresses. This process leads to nonuniform shrinkage across the package, creating asymmetric stress distribution and localized strain. Volumetric shrinkage occurring due to CTE mismatches throughout the entire molding and cooling process and are referred to as thermal shrinkages (Tan et al., 2013). Chemical aging is another phenomenon where continued crosslinking occurs in some reactive sites even after initial curing, which can also result in volume shrinkage (Chiu et al., 2011). The chemical shrinkage of the EMC due to polymerization can be estimated by characterization of cure kinetics of the EMC. The degree of conversion (DOC), denoted as α, quantifies the extent of cross-linking and the formation of a 3D polymer network. It reflects the progress of the curing reaction toward the fully cured state, as shown in Equation 1 (Chiu et al., 2011):

$$\alpha = \frac{H(t)}{H_u} \tag{1}$$

where $H(t)$ is the heat released by the cross-linking reaction up to time t and H_u is the ultimate heat of reaction. The material properties of the thermosetting polymer EMC, such as cure shrinkage and storage Young's modulus, strongly depend on its cure state, which is influenced by temperature and time. The heat of reaction, the rate of heat generation, and DOC can be characterized using differential scanning calorimetry (DSC). The heat flow measured by DSC is directly related to the DOC of the EMC. As the curing reaction progresses, the heat flow changes, and the extent of the curing process can be tracked. Kamal's autocatalytic model is applied to describe the curing behavior of EMCs and epoxy resins, as shown in Equation 2 (Kamal, 1974).

$$\frac{d\alpha}{dt} = \left[k_1 \exp\left(\frac{-Q_1}{RT}\right) + k_2 \exp\left(\frac{-Q_2}{RT}\right)\alpha^m\right](1-\alpha)^n \tag{2}$$

where m and n are the reaction order constants, k_1 and k_2 are the reaction rate constants, Q_1 and Q_2 are the activation energies, R is the universal gas constant, and T is the absolute temperature. The Kamal model provides several key parameters that describe the curing process:

a. Reaction order (m and n)
b. Rate constants (k_1 and k_2)
c. Activation energy (E_a)

These parameters are obtained by fitting the model to experimental DSC data. Kamal's model provides information on how the curing reaction progresses over time and temperature. This data can be used to estimate the evolution of chemical shrinkage throughout the curing process. The conversion rate verus time can be estimated and chemical shrinkage of EMC in its fully cured state can be used in process-dependent modeling for warpage prediction

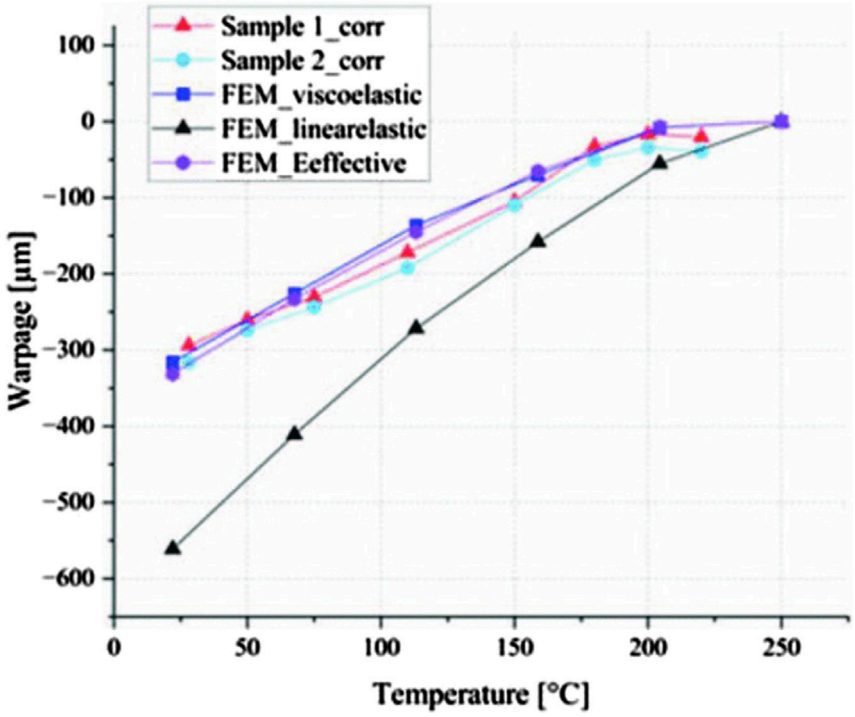

FIGURE 10
Comparison of experimental results to viscoelastic and effective elastic FEM model. Reprinted with permission from IEEE Proceedings (Huber et al., 2024).

using an initial strain approach (Cheng and Liu, 2019; Cheng et al., 2020; Yeh et al., 2015).

Another method for estimating cure-induced volumetric shrinkage is the P-V-T-C equations. The PVTC equation can be simply expressed as polynomials to describe the historical profiles of volume shrinkage under specified isothermal and isobaric states. PVTC equations describe how the specific volume of the EMC changes as a function of pressure, temperature, and degree of cure during the molding and curing processes. This allows accurate modeling of both the thermal and chemical shrinkage of the EMC during molding (Hong and Hwang, 2004; Chang et al., 2002).

Thermal mechanical analysis (TMA) instruments can characterize the chemical shrinkage of the epoxy molding compound during polymerization conversion and chemical aging. In the TMA method, the coefficient of thermal expansion is measured in-plane and out-of-plane over time and temperature (Chiu et al., 2011; Cheng and Liu, 2019).

2. Cure-dependent viscoelastic nature of EMC: The EMC exhibits time and temperature-dependent viscoelastic behavior during the curing process. The stresses that develop in the EMC do not immediately dissipate but gradually relax over time. The Prony series can effectively capture the time-dependent nature of the viscoelastic EMC, providing a good approximation of the relaxation Young's modulus (Yeh et al., 2015). This is a master function given by Equation 3 for the viscoelastic material in time domain can be described by using the generalized Maxwell spring-dashpot model. Prony series coefficients can be determined from experimental data obtained through dynamic mechanical analysis (DMA). The DMA method can be used to measure the relaxation Young's modulus of the substrate, mold compound, and underfill. Young's modulus is measured by applying a cyclical load at the centre of the sample in a temperature-controlled environment.

$$E(t,T,\alpha) = E(\xi, T_T, \alpha) = E_0(\alpha)\left[w_\infty(\alpha) + \sum_{i=1}^{N} w_i(\alpha)\exp\left(\frac{-\xi}{\tau_i(\alpha)}\right)\right] \quad (3)$$

where E is the cure-dependent relaxation Young's modulus, ξ is the reduced time or the pseudo-time, T and α are temperature and DOC respectively. E_0 is the glassy Young's modulus, N is the number of Maxwell elements, τ_i is the relaxation time, w_i is the weighting factor.

The Prony series parameters are input into the FEM software to define the viscoelastic material behavior. This allows the simulation to account for time-dependent stress relaxation and creep during the wafer packaging process. When combined with time-temperature superposition principles, Prony series can effectively model the temperature-dependent response of EMC during thermal cycles in wafer packaging process. The material properties of the EMC are strongly influenced by its glass transition temperature, T_g. Below T_g, the EMC is in a glassy state, exhibiting high stiffness and a low coefficient of thermal expansion. Above T_g, the EMC transitions to a rubbery state, resulting in a lower Young's modulus and a higher thermal expansion coefficient. The Williams, Landel, Ferry (WLF)

model can be used to describe how viscoelastic properties shift with temperature near T_g (Yeh et al., 2015). The WLF model, given by Equation 4, provides a method to design a master curve by horizontally shifting viscoelastic data obtained at various temperatures onto a single reference temperature. This is achieved using a shift factor, a_T, which adjusts the time scale to account for temperature changes.

$$\log_{10} a_T = \frac{C_1 (T - T_r)}{C_2 + (T - T_T)} \tag{4}$$

where T is the temperature and T_r is the reference temperature at which the master curve is constructed. C_1 and C_2 are empirical constants.

4.2 Analytical models to simulate residual stresses

4.2.1 Stoney's equations

In 1909, George Stoney investigated the deformation of a steel rule (substrate) with a thin metal film deposited on it through electrolysis. His research laid the groundwork for the famous Stoney equation, shown in Equation 5, which describes the relationship between the stress in the deposited film and the resulting curvature of the substrate (Stoney, 1909):

$$\sigma_f = \frac{h_s^2 E_s}{6Rh_f (1 - \nu_s)} \tag{5}$$

where σ is the stress, R is the radius of curvature, E is the Young's Young's modulus, h is the thickness, ν is the Poisson's ratio, and the subscripts f and s correspond to the film and substrate, respectively. Stoney's equation has been widely used to calculate residual stress by analyzing changes in wafer curvature. This provides a straightforward analytical approach for estimating warpage of systems with circular shapes, such as semiconductor wafers. The uniform spherical warpage of wafers can be described in terms of the warp, w, which is derived from simple geometry, as shown in Equation 6:

$$w \approx \frac{d^2}{8R} \tag{6}$$

where d is the wafer diameter, and R is the radius of curvature of the deformed wafer.

This adaptation made it widely applicable in the semiconductor manufacturing industry for analyzing wafer warpage. FEM models often use Stoney's equation as a reference point, with researchers comparing FEM results to Stoney's predictions to validate their models or highlight improvements (Schicker et al., 2016). The Stoney equation has limited applicability as it is only valid for cases where the substrate and film materials exhibit isotropic linear elastic behavior, the film thickness is significantly smaller than the substrate thickness, and the radius of curvature is much greater than the substrate thickness. Several studies have attempted to extend the scope of the Stoney formula by proposing modified versions that relax the assumptions of isotropic substrate materials (Janssen et al., 2008), the film thickness being much smaller compared to the substrate (Injeti and Annabattula, 2015), and the uniform film stress distribution (Qiang et al., 2021). Due to the involvement of different materials and complex geometries in heterogeneously integrated wafer assemblies, Stoney's equation becomes inadequate. It does not account for non-uniform stress distributions, non-linear material behavior, complex geometries, and multiple layers with varying properties (Ostrowicki et al., 2018).

4.2.2 Timoshenko's theory for bilayer materials

Timoshenko's analytical solutions for bi-material layers have been employed to investigate the CTE mismatch stresses in the multi-material layers of the wafer assembly. This approach enables a quick and reliable prediction of warpage in the reconstituted wafer (?) (Vellukunnel et al., 2023; Xing et al., 2015).

In a bilayer strip, a mechanical displacement occurs as a result of thermal changes within the interface as shown in Figure 11. Timoshenko's analysis provides a curvature and maximum deflection for this deformation as shown in Equations 7, 8 respectively (Vellukunnel et al., 2023):

$$\frac{1}{\rho} = \frac{(\alpha_2 - \alpha_1)\Delta T}{\frac{h}{2} + \frac{2}{h}(E_1 I_1 + E_2 I_2) * \left(\frac{1}{(E_1 a_1} + \frac{1}{E_2 a_2}\right)}, \tag{7}$$

$$\delta = \frac{l^2}{8\rho}. \tag{8}$$

where ρ is the radius of curvature, h is the total thickness of the bi-material strip. E_1, I_1, α_1 and a_1 are Young's modulus, moment of inertia, CTE and thickness of layer 1 respectively. E_2, I_2, α_2 and a_2 are the Young's modulus, moment of inertia, CTE and thickness of layer 2 respectively. δ is the warpage or the deformation along the perpendicular axis to the bi-material strip.

Effective material propertives of Young's modulus and CTE can be used to accurately represent multi-component layers for curvature estimation with Timoshenko's equations (Xing et al., 2015).

4.3 Numerical modelling approaches

FEM has been crucial in studying how different properties of the material affect the warpage and stress distribution. Multiphysics finite element modeling enables the simulation of coupled thermomechanical effects, accounting for both thermal stresses and mechanical deformations simultaneously.

FEM can incorporate nonlinear material behaviors, temperature-dependent properties, and viscoelastic effects, providing a more realistic representation of material responses. The viscoelastic properties of EMC play a crucial role in warpage behavior, especially at high temperatures. The functional group cross-linking reaction of EMC and its viscoelastic relaxation contribute to warpage during the reconstituted wafer process.

4.3.1 Process-dependent modeling methodology

FEM models can characterize the evolution of the warpage during a single or all processes by using process-dependent modeling methodologies. The warpage orientations of the reconstituted wafer can evolve from convex to concave bow shapes during the different processes of fan-out packaging, as shown in Figure 12. Process modeling techniques primarily involve

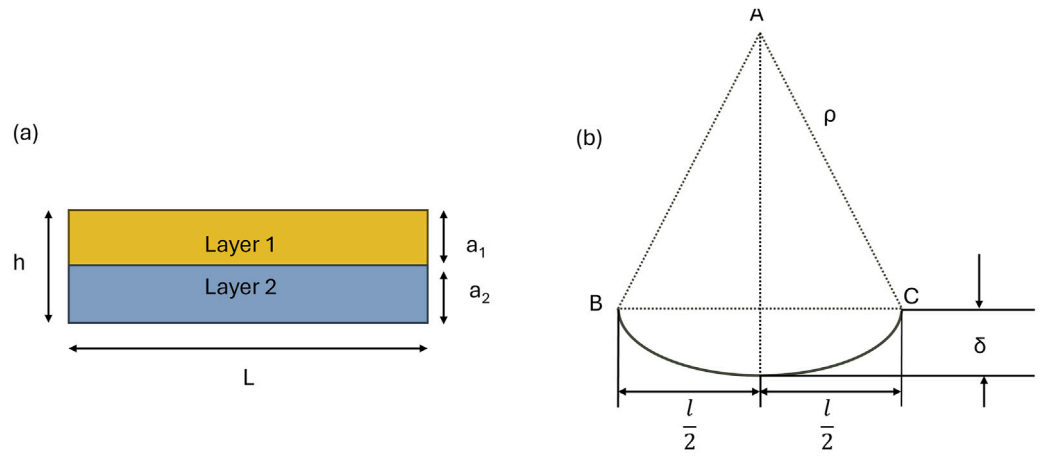

FIGURE 11
(A) Bilayer strip **(B)** Deflection of bilayer strip.

a thorough investigation of the temperature profiles in a real fan-out fabrication process. FEM models combine thermal and mechanical responses to represent the evolution of warpage induced by these temperature profiles. Coupled chemical-thermomechanical FEM models in which the cure kinetics and the cure-dependent viscoelastic behavior of EMC material have proven effective in this regard (Cheng et al., 2020; Yeh et al., 2015; Chiu et al., 2018).

ANSYS's element birth-and-death technique is a powerful approach used to model various stages of the FOWLP manufacturing process sequentially. This method selectively activates and deactivates different elements within the finite element model, accurately representing the different layers and materials involved. By manipulating the inclusion of elements such as the epoxy molding compound, carrier wafer, redistribution layers, and debonding materials, engineers can effectively model crucial stages such as compression molding, debonding, back grinding, and RDL fabrication. For example, during the simulation of the molding process, only the EMC layer and the carrier are active, while other components remain inactive. Back grinding can be modeled by deactivating certain parts of the EMC layer, simulating the removal of excess material. As RDL layers are created, their corresponding elements are activated in sequence, mimicking the build-up process. This technique provides valuable insight into thermal management and potential reliability issues throughout the FOWLP manufacturing sequence. Proper selection of elements and consideration of residual stresses from previous stages are crucial to a accurate representation of the physical process. Validating the model with experimental data at key stages helps ensure accuracy, enabling engineers to gain insight into the FOWLP process and optimize process and material properties (Xing et al., 2015; Cheng and Liu, 2019; Wu and Lan, 2019).

The nonaxisymmetric or asymmetric warpage behavior of reconstituted wafers can be modeled by incorporating nonlinear finite element analysis and the impact of gravity in process-dependent FEM simulations (Cheng and Liu, 2019; Cheng et al., 2020).

Coupled explicit dynamic and static models can address transient and steady-state events during the fan-out process, such as grinding on the backside where the excess EMC is removed by a grinding wheel to reduce overall package thickness and weight. Wafer stiffness is often unable to support grinding stress on the surface and warpage can occur. To analyze the grinding stress on silicon wafers during the back-side grinding process, a finite element model is established by setting dynamic loads and contact conditions. An explicit dynamic model is used to simulate the relationship between the grinding wheel and the silicon wafer. A static model is incorporated with the explicit dynamic model to predict the wafer warpage grinding stress on the damaged layer of the silicon wafer. This method provides valuable information regarding the grinding wheel rotation speed, the wafer rotation speed, and the feed rate effectively control the wafer warpage (Wu et al., 2023; Wu and Wong, 2024).

4.3.2 Material representation through homogenization methods

Fabrication of RDL layers involving PI passivation and electroplating of copper layers can induce warpage. Each step in the RDL fabrication process, including deposition, patterning, and curing of the dielectric and metal layers, introduces stress into the wafer structure. Warpage is primarily caused by mismatches in the thermal expansion coefficient (CTE) between the deposited materials, with electrochemically deposited Cu traces substantially contributing to the total warpage due to the CTE mismatch and plastic deformation (Zhu et al., 2014). The high aspect ratios of the Cu traces in the RDL layers can face issue meshing in FEM software. To simplify modeling of complex Cu traces, pads, vias, and dielectric layers, we approximated these layers as equivalent homogeneous medium and evaluated their effective properties. Trace mapping methods have also been used to simplify cu traces in packages.

Homogenization techniques have been applied to approximate the complex layout of redistribution layers, which consist of a mixture of copper and polyimide in varying proportions on a carrier substrate in the RDL-first approach. Rule of mixtures has

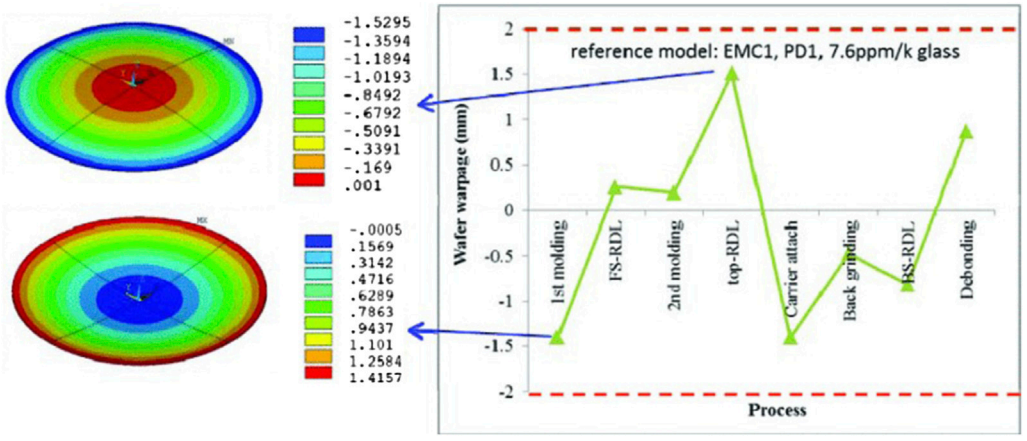

FIGURE 12
Simulation of warpage trend during Fan-out manufacturing. Reprinted with permission from IEEE Proceedings (Chong et al., 2020).

been employed to determine the effective properties, such as the elastic modulus and the coefficient of thermal expansion, of the RDL layers comprising both copper and PI. This approach helps to account for the influence of these constituent materials on the overall warpage behavior (Huber et al., 2024).

4.3.3 Parametric analysis

Parametric analysis in conjunction with Finite Element Method (FEM) has been extensively used to understand dominating factors and process conditions for wafer warpage simulation in FOWLP. This approach involves systematically varying key parameters such as material properties (e.g., viscoelastic properties of Epoxy Molding Compound and Polyimide) (Hu et al., 2023; Hamaguchi et al., 2016), geometric dimensions (e.g., die size and thickness) (Hu Z. et al., 2021; Wu and Lan, 2019), and process conditions (e.g., temperature profiles during curing) (Sanchez et al., 2022). These studies have provided valuable information on the factors that influence warpage, enabling quantitative relationships to be established between various parameters and warpage outcomes. This methodology has proven crucial for the optimization of the design, sensitivity analysis, and process improvement in FOWLP, ultimately guiding material selection and fabrication processes to minimize warpage in semiconductor packaging.

4.3.4 AI/ML models

Recent research has explored artificial intelligence and machine learning approaches to predict warpage in fan-out wafer-level packaging. The complexity arising from temperature- and time-dependent material behavior in fan-out wafer assembly makes it challenging to develop comprehensive analytical models for warpage prediction, while FEM models prove computationally intensive and cost-prohibitive.

Several studies have employed FEM simulations to generate warpage datasets for various package geometries, subsequently using these to train machine learning models (Chen and Wu, 2024). demonstrated how traditional analytical approaches such as Stoney's equations could be combined with data-driven techniques to improve warpage prediction, even when models deviate from the assumptions of Stoney's equation. Their artificial neural network (ANN) specifically predicts correction factors applied to the Stoney equation, accounting for real-world packaging complexities that the original equation cannot address.

Convolutional Neural Networks (CNNs) have successfully mapped relationships between package geometry and warpage, with edge detection techniques enhancing training efficiency (Wang et al., 2021; Liu et al., 2020). However, these approaches typically rely on simplified FEM models using equivalent thermal expansion coefficient methods to approximate the EMC behavior, limiting their application to specific FOWLP processes.

Physics-based machine learning approaches have emerged to address the "black-box" nature of neural networks. Yao et al. (2022) developed a physics-based ANN model that incorporates physical governing equations to account for the viscoelastic nature of EMC. Their two-stage approach first employs a material ANN surrogate model processing raw material properties to predict Prony series and WLF parameters, followed by a mechanical ANN model using these outputs to predict package mechanical response. Although this method demonstrated high reliability with FEM results and improved accuracy with increasing training samples, it assumed elastic, isotropic, and temperature-dependent behavior for other constituent materials.

These approaches face several limitations. Complex or unique packaging configurations not represented in the training data may yield unreliable predictions. Additionally, significant computational resources are required for training and implementation, while the simplified material behavior assumptions may not fully capture real-world complexity.

In addition to 'fitting' models to predict warpage, AI/ML models have also been shown to reduce the dependence on expensive testing and metrology instruments for material characterization in electronic assemblies (Stoyanov and Bailey, 2022).

4.3.5 Multi-scale approaches

Predicting warpage and stress across a wafer during fan-out wafer-level packaging processes with finite element analysis requires accurate prediction the behavior of the physical structures of the wafer containing semiconductor chips and redistribution layers. Given the extreme length scales and aspect ratios of these

structures, a full finite element method is infeasible. Multiscale techniques can employ modeling techniques that can be classified as (1) material homogenization (as detailed above), (2) representative volume elements (RVE), and (3) domain decomposition models to overcome these restrictions.

Material homogenization uses algebraic equations to approximate mechanical properties (Young's modulus, the Poisson's ratio and the CTE) in local areas based on the mixture rule (as discussed in 4.3.2 above). RVE homogenization is a technique used to predict the equivalent material properties of unit cells representative of the periodic repetition of the heterogeneous composite structures at a local level. Each unit cell will contain the geometry and material properties of the original structures, and with appropriate boundary conditions a finite element analysis is undertaken to predict the equivalent material properties and stiffness matrix for a homogenized unit cell. Both techniques provide the ability to significantly reduce the complexity of the model, and hence reduce mesh sizes in a process model using finite element analysis. Domain decomposition models solve the governing equations for wafer warpage by splitting the structure into smaller sub-domains and iterating between these subdomains until convergence. Such a technique generally keeps the heterogeneous structure of the original wafer intact and can be exploited on parallel computers for faster computation.

The element birth-and-death technique is used to predict the warpage in which materials are added and subtracted at each step of the process. Using this with the rule of mixtures to approximate heterogeneous material properties locally, a finite element simulation and a finite element analysis can be undertaken. This modeling approach has been used with response surface methodology for parametric analysis to investigate the impact of copper volume fraction in RDL layers and CTE of the glass carrier wafer (Yu et al., 2022). The differences between predicted and measured warpage ranged from 2%–15% for each of the processes. Optimal values for glass CTE and Cu volume fraction in the RDL layer were 3.61 ppm and 20%, respectively. These optimal values reduced the overall warpage by 36% after all the process steps were completed. Comparisons between material homogenization and RVE approaches demonstrated that the RVE approach is more accurate in predicting process-induced warpage where predictions of the final warpage are experimental (273um), material homogenization (369um) and RVE (305um) (Duan et al., 2023). The vast majority of published papers for predicting wafer warpage use either material homogenization or RVE approaches. Although domain decomposition has been widely used for predicting mechanical behavior of composite structures in other fields, it has received very limited applications for use in wafer warpage predictions (Roqueta et al., 2024). Subsequent analysis has shown that using a domain decomposition approach can yield results of similar accuracy to a full finite element calculation for wafer warpage predictions with significant computational cost savings (Roqueta et al., 2024).

At present, there is no consensus on a standard numerical approach to use to predict wafer warpage during each processing step of a wafer-level packaging process. Various modeling approaches have been reported in the literature as discussed above to address this complex nonlinear, multi-material, multi-physics, and multi-scale analysis. Further research is required to access these approaches in terms of balancing prediction accuracy and computational resources required to undertake detailed parametric analysis. At the design stage, accuracy and parametric analysis to identify optimal package designs and unit process conditions is a key requirement. During the actual manufacturing process, the ultimate goal is the development of digital twins for each process step that combines data gathered from sensors and fast real-time models that can support process control to minimize warpage throughout the whole wafer packaging process.

5 Controlling warpage

The following options are reported as key factors for controlling warpage in FOWLP processes.

5.1 Material properties

Optimizing thermal and mechanical properties of the materials used throughout the FOWLP processes can address warpage. For instance, three key properties are:

1. Coefficient of Thermal Expansion (CTE): Selecting materials with closely matching temperature-dependent CTE in the reconstituted wafer stack can greatly minimize warpage. The CTE values of EMC and carrier wafer are particularly critical when it comes to minimizing warpage (Salahouelhadj et al., 2018). The Young's modulus and CTE of EMC before the glass transition temperature (T_g) have been found to significantly affect warpage. Decreasing the CTE of EMC before T_g can significantly reduce warpage (Hu et al., 2023). Using carrier wafers with higher CTE and Young's modulus can mitigate warpage by providing structural stability during processing (Hu Z. et al., 2021).
2. Glass Transition Temperature (T_g): Using an EMC material with T_g higher than the PMC temperature can reduce the warpage of the molded wafers (Salahouelhadj et al., 2018). The warpage of the wafer can be reduced by increasing the glass transition temperature (T_g) of the molding compound because the CTE of the EMC decreases with increasing T_g (Kwon et al., 2017).
3. Young's modulus: Reducing the Young's modulus of EMC can reduce the warpage of molded wafers due to lower stress relaxation (Salahouelhadj et al., 2018; Kwon et al., 2017). CTE and Young's modulus are most often inversely related, therefore a balance is required (Hamaguchi et al., 2016).

5.2 Process parameters

1. Temperature: Warpage is influenced by the thermal history of the wafer, so controlling the temperature profile during processing can reduce the warpage effects. Temperature higher than T_g of the EMC during the fan-out process is a major cause of warpage, as CTE increases considerably after T_g. The curing of the dielectric polymer at high temperatures

can cause warpage and damage to the EMC. Therefore, it is necessary to use dielectric polymers with curing temperatures below 200 deg C in the fan-out process (Yamamoto et al., 2018). Additional time-controlled thermal treatments can be provided during the fan-out manufacturing process to adjust warpage (Stegmaier et al., 2023; Sanchez et al., 2022).

2. Mold Cure-rate: Ensuring uniform curing of EMC can lead to more balanced stress distribution across the wafer or panel. Young's modulus and cure-induced chemical shrinkage of the EMC material during the molding process are directly proportional to their time- and temperature-dependent cure state (Cheng et al., 2020). To prevent incomplete curing and intrinsic defects common to conventional EMCs, embedding dies within novel thermosetting films together with thermal annealing techniques can help manage residual stresses that contribute to warpage (Li and Yu, 2022). Ultraviolet (UV) curable EMC can be used instead of traditional thermally curable EMC, ensuring rapid curing at room temperature and faster process flows for both FOWLP and FOPLP (Schindler et al., 2024).
3. Mold flow rate: Molding materials used for fan-out wafer and panel-level processes should display a low cure temperature, low chemical shrinkage, and match thermomechanical properties whilst maintaining a suitable flow-ability to ensure low warpage of molded wafers. The dispensing of liquid EMC has the highest risk of incomplete and non-homogeneous filling associated with low flowability and longer flow lengths in large cavities during compression molding (Braun et al., 2015; Kwon et al., 2017).

5.3 Geometry

1. Layer Thickness: Adjusting the thickness of various layers can help control warpage. For example, reducing the EMC thickness and increasing the carrier thickness can lead to reduced warpage. Experimental and simulation-based design of experiments (DoE) have shown that increasing die thickness and reducing the thickness of the molding layer over a die during wafer reconstitution can reduce warpage (Wu and Lan, 2019; Gadhiya et al., 2019; Salahouelhadj et al., 2018).
2. Chip Geometry: Reducing the area of dies in reconstituted wafers, while increasing thickness, can help mitigate warpage (Wu and Lan, 2019). Increasing thickness of dies effectively reduces the CTE of the EMC and hence this can reduce warpage. The smaller CTE of the chips becomes more dominant when the thickness of the die is increased (Wu and Lan, 2019; Hu Z. et al., 2021).
3. Chip layout on Reconstituted Wafer: The asymmetric layout of the chips on the wafer can lead to saddle-shaped warpage (Wu and Lan, 2019). In addition, increasing the spacing of the chips in the wafer has been reported to result in increased wafer warpage (Hu Z. et al., 2021).
4. Redistribution Layer (RDL): The design of RDLs, including their thickness and material composition, plays a role in controlling warpage (Ostrowicki et al., 2018). An increase in the number of RDLs leads to a decrease in warpage,due to increased stiffness of the reconstituted fan-out wafer. Also, the number of RDL layers has a stronger influence on the influence on warpage when the copper content within the RDLs increases. The effective Young's modulus of the RDL layer increases with increases in copper content, while there is no significant change to CTE. This improves the ability of the wafer to resist heat-induced deformations (Hu W.-L. et al., 2021)

By implementing a combination of these methods, manufacturers can effectively manage and reduce warpage in FOWLP processes, leading to more reliable and cost-efficient system-in-package (SiP) solutions. The most optimal approach may vary depending on the specific package design, materials used, and application requirements.

6 Conclusions and future trends

This paper provided a review of the current state-of-the-art in measuring warpage, predicting warpage, and methodologies suggested for controlling warpage during different stages of the fan-out manufacturing process. Measurement techniques such as shadow moire, digital fringe projection, and digital image correlation provide insight into the levels of warpage being produced due to thermal excursions during the build-up process as well as deformation/stain maps across the wafer. These techniques provide valuable data for model verification and validation. Finite element modeling using temperature-dependent material data and nonlinear constitutive laws (e.g., viscoelasticity for polymer materials) is a powerful modeling technique for predicting warpage for these thin-film structures. Machine learning also provides a powerful prediction method based on the training data provided.

Although much progress has been made in this field, warpage is still a significant challenge as semiconductor packages require more redistribution layers and high-density interconnect line/spacing to accommodate higher I/O and bandwidth especially for HPC and AI applications. Challenges that need to be addressed include:

- Need for Materials Data and Failure Criteria: The need for accurate temperature- and cure-dependent materials is a key to thin-film structures in fan-out packaging. Additionally, a thorough understanding of the adhesion strength of the RDL layers is required at these very small dimensions.
- Need for Multi-Scale Models: A full finite-element model of the wafer with the semiconductor components and packaging structures (RDL, etc.) has extreme aspect ratios and would require significant compute times. Accurate and standardized multiscale modeling techniques are required to address this computational complexity to support package design and unit process optimization in terms of minimizing warpage at the package design stage.
- Need for Digital Twins: As detailed above, full parametric and sensitivity analysis of the design space requires fast predictions. Machine learning with appropriate training data (e.g., from

physics models as detailed above) or response surface models provides an opportunity to develop this capability. Digital twins (with fast model predictions) using data from sensors placed in each process measuring key process parameters that impact warpage provide an opportunity to control warpage during the wafer-level packaging process.

Author contributions

PP: Writing–original draft. CB: Writing–review and editing.

Funding

The author(s) declare that financial support was received for the research, authorship, and/or publication of this article. Authors acknowledges the financial support from Arizona State University for this PhD study into modelling and controlling warpage in the fan-out wafer-level packaging process.

Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Generative AI statement

The author(s) declare that no Generative AI was used in the creation of this manuscript.

Publisher's note

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frontiers | Frontiers in Materials

TYPE Original Research
PUBLISHED 26 March 2025
DOI 10.3389/fmats.2025.1581900

OPEN ACCESS

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RECEIVED 23 February 2025
ACCEPTED 13 March 2025
PUBLISHED 26 March 2025

CITATION
Yao X, Tian S, Zhou M, Jiao H, Wang J and Wang B (2025) Microstructure, interfacial reaction and shearing property of Sn-58Bi solder joints reinforced by Zn particles during isothermal aging.
Front. Mater. 12:1581900.
doi: 10.3389/fmats.2025.1581900

Microstructure, interfacial reaction and shearing property of Sn-58Bi solder joints reinforced by Zn particles during isothermal aging

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In this paper, micro-sized Zn particles were added into Sn-58Bi solder flux to form Sn-58Bi-xZn composite solder. The evolution of microstructure, interfacial IMCs and shearing properties during long-term aging were investigated. The wettability of Sn-58Bi-xZn solder decreased with the increase in Zn content. Adding the Zn element refined the microstructure of Sn-58Bi solder and mitigated the aggregation of Bi phases during aging. The interfacial IMCs changed from Cu_6Sn_5 to $Cu_6(Sn,Zn)_5$ with 0.5 wt% Zn addition. Further increasing the Zn content, Cu_5Zn_8 instead of $Cu_6(Sn,Zn)_5$ generated at the Sn-58Bi-2.0Zn/Cu interface. After long-term aging, Bi diffused into Cu_3Sn and formed an aggregation layer. With 0.5 wt% Zn addition the growth of interfacial Cu_6Sn_5 IMCs was suppressed. Shearing tests were conducted to evaluate the mechanical properties of Sn-58Bi-xZn joints before and after aging. Aging and excess Zn addition lead to a decrease in the shearing force of the joints. The fracture mode changed from solder fracture to interface fracture with excess Zn addition The Sn-58Bi-0.5Zn solder joints exhibited the optimal shearing properties during aging. The optimum amount of Zn addition to Sn-58Bi solder was 0.5 wt%.

KEYWORDS

Sn-58Bi, Zn addition, interfacial IMCs, shearing properties, aging

1 Introduction

Tin-lead solders have been widely used in the electronic packaging industry for decades. Due to the toxicity of lead and the increasing environmental concern, lead-containing solder has been banned since the ROSH Directive was enacted in 2006 (Zhang and Tu, 2014). Currently, several Pb-free solders such as Sn-Ag, Sn-Cu, Sn-Ag-Cu, Sn-Bi and Sn-Zn solder alloys have been extensively developed to replace the traditional Sn-Pb eutectic solder. Nevertheless, some application and reliability issues still need to be overcome (Abtew and Selvaduray, 2000). For example, the melting temperature of Sn-Ag, Sn-Cu and Sn-Ag-Cu solder alloys are too high to be compatible with printed circuit board (PCB) substrates during the soldering

process. Moreover, the excessive growth of Cu_6Sn_5 and Ag_3Sn intermetallic compounds (IMCs) in service will gradually reduce the reliability of solder joints (Berger et al., 2023; Mu et al., 2012; Zhang et al., 2024). The easy oxidation and poor wettability characteristics of Sn-Zn solder alloy hindered its application in the electronic industry (Liu et al., 2015; Xue et al., 2016).

Sn-Bi solder with its good solderability as the eutectic Sn-Pb solder, superior ultimate tensile strength and yield strength has drawn attention as an attractive candidate solder. However, the poor ductility and low reliability of Sn-Bi solder joints need to be improved (Zhang et al., 2022; Li et al., 2020). In recent years, reinforcement of solder alloys with micro or nanoparticles has been adopted to improve the performance of Sn-Bi alloy and is currently receiving great attention. The addition of micro Ni-particles significantly refined the microstructure of Sn-58Bi solder. Ni-Sn intermetallics obstructed the movement of Bi atom diffusion and improved the electromigration resistance of the Sn-58Bi composite solder joints (Xu et al., 2011). Li and Chan, (2015) have studied the mechanical properties and the growth of IMCs at the solder/Cu interface of Sn-58Bi solder with Ag nanoparticles addition. The results showed that the microhardness was increased by 12.2% and the shear strength was enhanced by 18.9% for the as-prepared solder. The dispersion strengthening theory was employed to elaborate the mechanical improvement mechanism. Some nanoparticles of non-metallic such as TiO_2 (Tsao et al., 2012), CNT (Shen et al., 2013; Sun et al., 2016; Sun et al., 2022), POSS (Zhang et al., 2010; Rashid et al., 2009), graphene (Yang et al., 2013; Ma et al., 2017; Peng and Deng, 2015), Al_2O_3 (Hu et al., 2015) have been added into Sn-Bi alloy. These particles can accelerate β-Sn heterogeneous nucleation during reflow and reduce the size of β-Sn significantly. The growth of interfacial IMCs was depressed with nano non-metallic particle addition. However, these particles could not have metallurgical bonding with Sn solder. The excessive non-metallic particles will reduce the wettability due to the poor fluidity of composite solder (Yang et al., 2009).

Presently, most of the research is focused on the microstructure and mechanical properties of nanoparticle composite solder alloy itself, and few of them have studied the reliability of the micro joints using nanoparticle composite solder. Accordingly, this study aims to investigate the microstructure and mechanical properties of Sn-58Bi solder bearing micro-sized Zn-particles and prepare the ball grid array (BGA) solder joints using this composite solder alloy. The shearing test was conducted to evaluate the reliability of the solder joints. The effect of micro-sized Zn particles addition and solid-state aging on the reliability of Sn-58Bi micro-sized Zn particles composite solder joints was investigated.

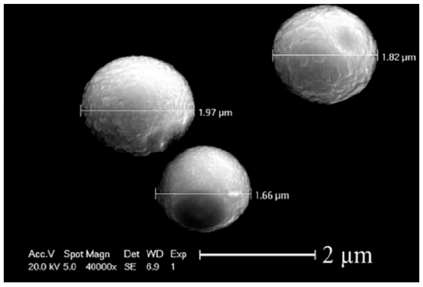

FIGURE 1
Morphology of spherical pure Zn particles.

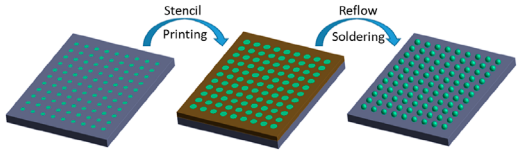

FIGURE 2
Preparation schematic diagram of composite solder joints.

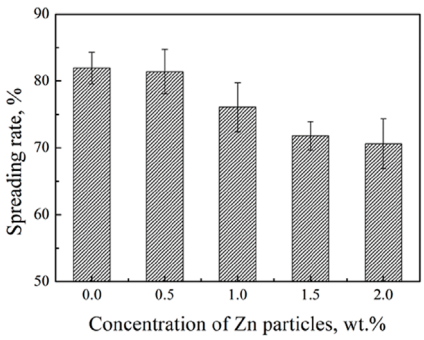

FIGURE 3
Spreading rate of the Sn-58Bi-xZn composite solder paste.

2 Experimental procedures

2.1 Composite solder joints preparation

Commercial Sn-58Bi solder paste with 11.5 wt% flux was used as the base material. The Sn-58Bi-xZn micro particles composite solder paste was prepared by mechanically dispersing the micro-sized Zn-particles into the Sn-58Bi solder paste. The spherical pure Zn particles with about 2.0 μm diameter were shown in Figure 1, and the content of Zn particles was set as 0, 0.5, 1.0, 1.5 and 2.0 wt% respectively. The mixed solder paste was stirred primarily under vacuum condition for at least 1 h to ensure the uniform distribution of Zn particles. Then, the composite solder paste was printed by a stainless steel stencil with a 1.2 mm diameter and 1 mm thickness. The printed circuit board (PCB) with a 0.8 mm diameter Cu pad was used as the substrate. Before soldering, Cu pads were cleaned by a 4.0 wt% HCl solution. The composite solder joints were heated on a heating platform at 180 °C for 40 s. After soldering, the joints were air-cooled and cleaned with alcohol as shown in Figure 2. The diameters of solder balls were about 1.0 mm.

2.2 Solid-state aging and shearing test

The as-soldered joints were solid-state aged by oil bath at 120°C for 10, 20, 30, 40 and 50 days. The average thickness of

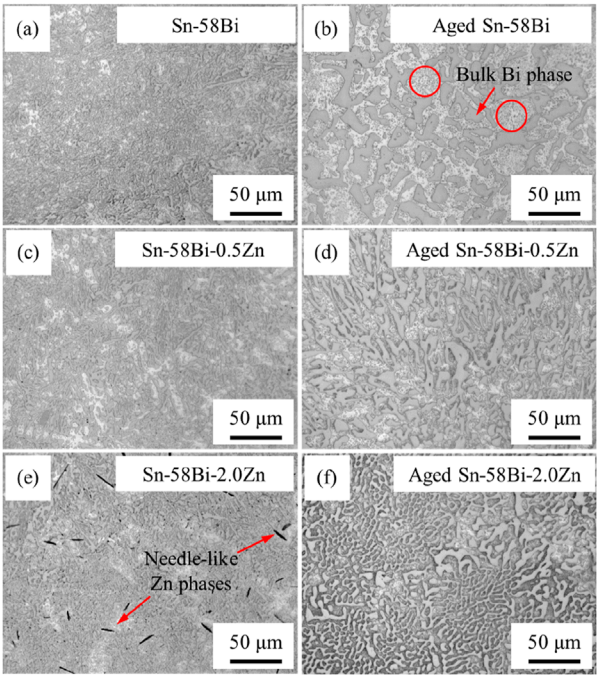

FIGURE 4
Optical microstructure of the solder bumps aged for 0 days and 40 days. **(a, b)** Sn-58Bi, **(c, d)** Sn-58Bi-0.5Zn, **(e, f)** Sn-58Bi-2.0Zn.

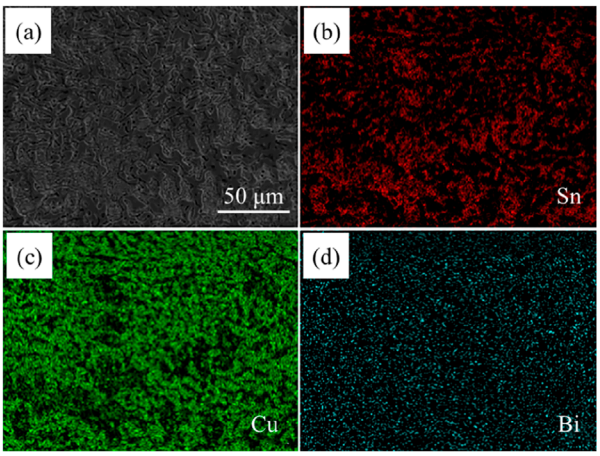

FIGURE 5
Element mapping of the as-soldered Sn-58Bi-0.5Zn solder alloy. **(a)** Microstructure of the alloy **(b)** Sn element **(c)** Bi element and **(d)** Zn element.

interfacial IMCs was calculated by measuring the total area of the IMCs and dividing it by the total length of the images. The mechanical properties of Zn-particles composite solder joints were evaluated by a shearing tester. The shearing force was calculated as an average of 20 solder joints with a shearing speed of 0.01 mm/s.

2.3 Wettability test

The wettability of composite solder paste was evaluated according to the standard of JIS-Z3198-3. A certain quality of composite solder paste was printed on a polished Cu substrate as well as a stainless steel substrate by the stencil printing method. Then, the samples were heated at 180°C for 60 s. The height of solder balls wetted on stainless steel substrate and Cu substrate was measured by screw micrometer. The wettability of composite solder paste was evaluated by the spreading rate S, which can be expressed as Equation 1:

$$S = \frac{D - H}{D} \times 100\% \quad (1)$$

Where S is the spreading rate of composite solder paste, D is the height of composite solder paste wetted on a stainless steel substrate, and H is the height of composite solder paste wetted on a Cu substrate.

2.4 Microstructure characterization

To characterize the microstructure, the solder joints were mounted in resin and ground using different grit sizes of emery papers. Finally, the samples were polished with 3.0, 0.5 μm diamond powder and 0.05 μm silica suspension. The specimens were etched with a solution of 4 vol% HNO3 + 96 vol% C2H5OH. The microstructure of composite solder matrix, interfacial IMCs and fracture surfaces after the shearing test was observed using a scanning electron microscope (SEM) equipped with an energy dispersive X-ray spectrometer (EDS).

3 Results and discussion

3.1 Wettability of the Sn-58Bi-xZn composite solder paste

The wettability is the primary condition for the usability of lead-free solder. Figure 3 presents the spreading rate of the Sn-58Bi-xZn composite solder paste on Cu substrates. The Sn-58Bi solder paste showed satisfactory wettability and the spreading rate was 81.9%. The spreading rate of the composite solder paste decreased slightly when 0.5 wt% Zn particles were added into the Sn-58Bi solder paste. Moreover, the spreading rate decreased seriously with more Zn particles addition. Residual Zn particles can be observed around the solder caps after soldering. It is worth noting that the molten solder and the Cu are assumed to be fully covered by flux. The wettability of solder on Cu is reactive wettability. The wettability was affected by the formation of interfacial IMCs. Different from Sn-Bi-Zn ternary alloy, the Sn-58Bi solder flux needs time to absorb the Zn particles. Due to the high cooling rate, excess Zn particles were not yet absorbed by the molten Sn-58Bi solder and existed at the edge of the solder cap. The aggregation of Zn particles hindered the spreading of molten solder on Cu. Therefore, the wettability deteriorated with the increase of Zn particles content.

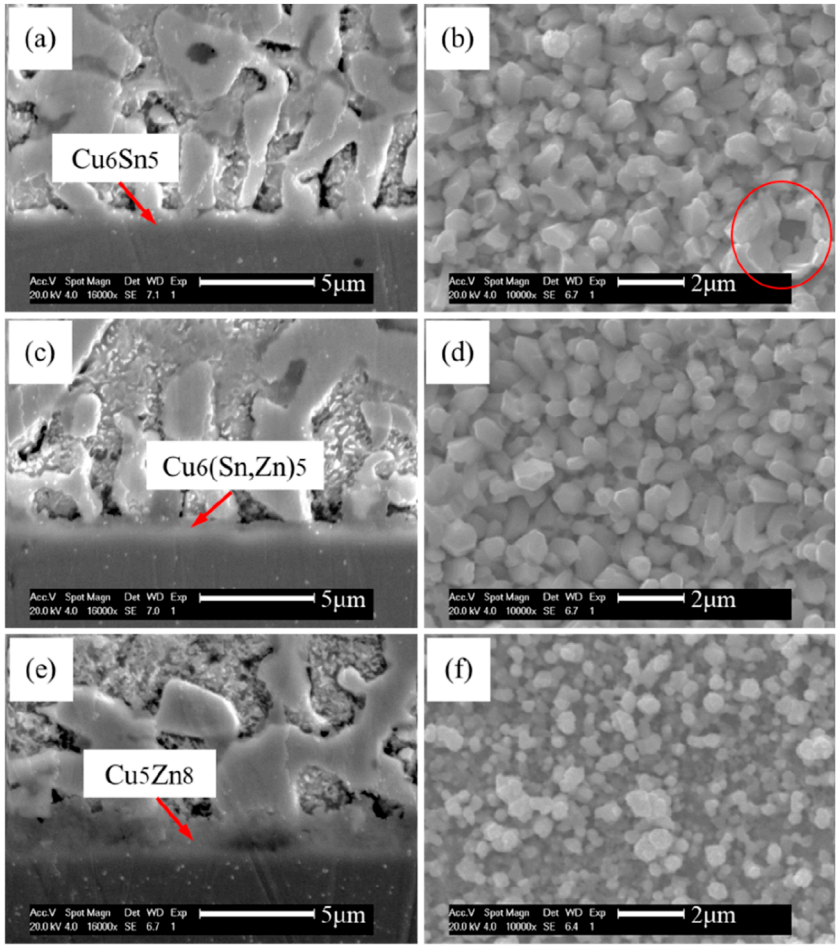

FIGURE 6
Cross-section and top-view microstructure of the initial IMCs at the interface. **(a, b)** Sn-58Bi/Cu, **(c, e)** Sn-58Bi-0.5Zn/Cu, **(e, f)** Sn-58Bi-2.0Zn/Cu.

3.2 Microstructure evolution of the Sn-58Bi-xZn solder bump during aging

Figure 4 shows the microstructure evolution of the as-soldered and aged composite solder bumps. The as-soldered Sn-58Bi solder bump shows a lamellar structure which mainly consists of Sn-rich phase and Bi-rich phase as shown in Figure 4a. With the addition of 0.5 wt% Zn particles, the microstructure of the composite Sn-58Bi-0.5Zn bump became finer with smaller Sn-rich phase and Bi-rich phase by comparing with the Sn-58Bi bump, as shown in Figure 4c. Fine Zn particles can be observed in the composite solder bump matrix.

Figure 5 shows the distribution of the Zn element in the as-soldered Sn-58Bi-0.5Zn composite solder bump. It can be found that Zn particles were uniformly distributed in the Sn-rich phase. According to previous studies (Ma and Wu, 2016; Shen et al., 2014), no binary or ternary compounds will form in the Sn-Bi-Zn ternary system. The existence of Zn particles played the role of refining the composite alloy by heterogeneous nucleation. The microstructure of the Sn-58Bi bump was not further refined with more Zn particles addition, as shown in Figure 4e. When the Zn content increased to 2.0 wt%, needle-like Zn phases can be found in the bump. It is reported that the ultimate tensile strength of Sn-Bi alloy was improved by the existence of needle-like Zn phases. However, the elongation of Sn-Bi-Zn alloy deteriorated seriously due to the high aspect ratio Zn phases (Shen et al., 2014). The tensile strength and shearing strength of Sn-58Bi alloy is much higher than that of Sn-37 Pb alloy (Abtew and Selvaduray, 2000). It is the poor ductility of the Sn-58Bi alloy that limits its utilization. Many efforts have been made on this problem, but it has not been solved until now (Zhang et al., 2022; Li et al., 2020; Xu et al., 2011).

The microstructure of the Sn-58Bi bump became coarse after aging for 40 days, as shown in Figure 4b. The bulk Bi phases were separately distributed in the Sn matrix. Some Bi phases with small size were observed as illustrated by the red circles in Figure 4b. The Bi phase in the bumps with Zn addition slightly grew after aging, as shown in Figures 4d, f. The microstructure of the Sn-Bi-Zn bumps kept a lamellar structure after aging for 40 days. The addition of Zn mitigated the aggregation and growth of Bi phases. The solute atoms migration is significant during thermal aging in the binary system, such as Sn-Pb, Sn-Bi and Sn-Cu, etc (Philippe and Voorhees, 2013). Based on the Ostwald ripening, the smaller second phases will dissolve and the larger ones will grow due to the diffusion of the solute atoms. The radius of the second

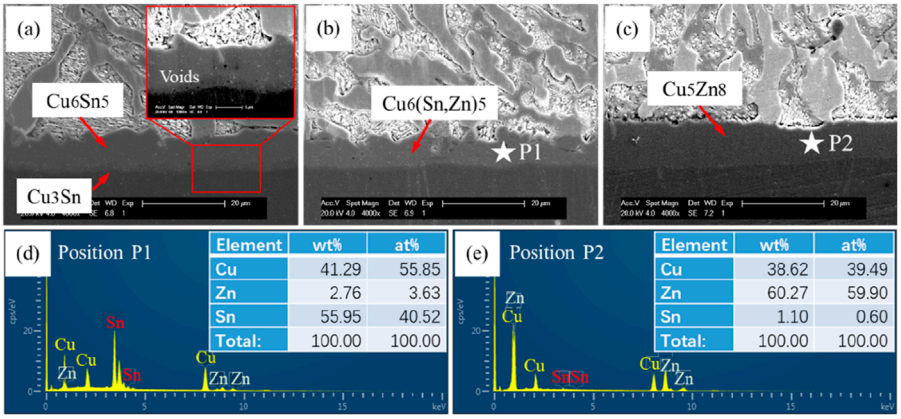

FIGURE 7
Microstructure and composition of the IMCs aged for 40 days. **(a)** Sn-58Bi/Cu interface, **(b)** Sn-58Bi-0.5Zn/Cu interface, **(c)** Sn-58Bi-2.0Zn/Cu interface, **(d)** element compositions at position P1 and **(e)** element compositions at position P2.

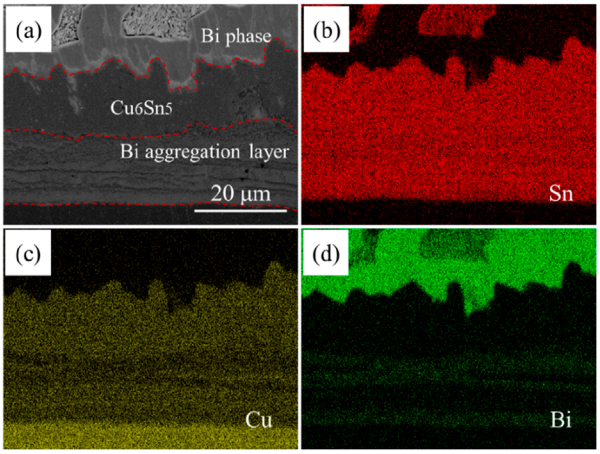

FIGURE 8
Layered Bi aggregation in the IMCs at the interface after aging for 50 days. **(a)** Microstructure of Bi-rich layer, **(b)** Sn element, **(c)** Cu element and **(d)** Bi element.

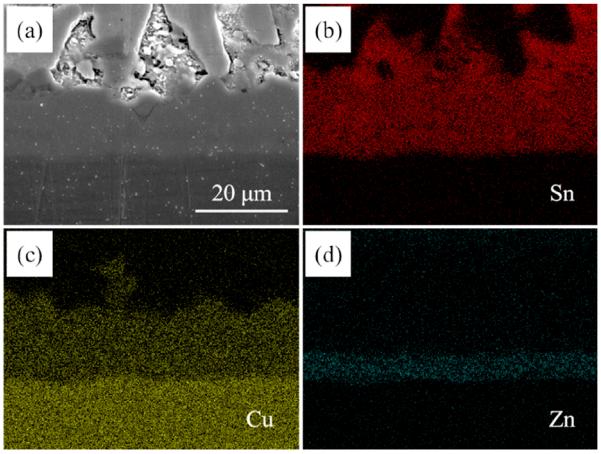

FIGURE 9
Element mapping at the Sn-58Bi-0.5Zn/Cu interface aged for 50 days. **(a)** Microstructure, **(b)** Sn element, **(c)** Cu element and **(d)** Bi element.

phase can be expressed as Equation 2 (Kim and Voorhees, 2018; Lifshitz and Slyozov, 1961),

$$r^3 = r_0{}^3 + K_0 t = r_0{}^3 + \frac{8D\gamma C_e \Omega^2}{9RT} t \quad (2)$$

where r is the radius of the second phase, r_0 is the initial radius of the second phase at the initial stage, K_0 is the coarsening rate, t is the aging time, D is the diffusivity of solute atoms in the matrix, γ is the interface energy, Ce is the equilibrium concentration of solute atoms around the large second phase, Ω is the molar volume, R is the gas constant, T is the aging temperature.

According to the Sn-Zn binary alloy phase diagram, the solubility of Zn in Sn is approximately 0.7 at% at eutectic temperature (Wu et al., 2024). Due to the small volume and high undercooling of Sn-58Bi-xZn solder balls, zinc was not precipitated from Sn during the cooling process, resulting in the formation of supersaturated solid solutions. The solid solution atoms will hinder the intragranular diffusion of Bi in Sn leading to the decrease of diffusivity of solute atoms (Delhaise et al., 2019). Therefore, the radius of the Bi phase in the Sn matrix with Zn addition decreased after thermal aging.

3.3 Microstructure evolution of interfacial IMCs during aging

The microstructure of the as-soldered solder/Cu interfaces is shown in Figure 6. The interfacial IMCs were observed from a cross-sectional view and top-view respectively. An extremely thin and scallop-shaped interfacial IMCs layer formed at the Sn-58Bi/Cu interface as shown in Figure 6a. According to the previous studies (Jeong et al., 2023; Chen et al., 2018; Hao et al., 2024), the composition of the IMCs was Cu_6Sn_5. The diameter of the IMCs was about 1.5 μm which can be observed from the top-view. Defects can

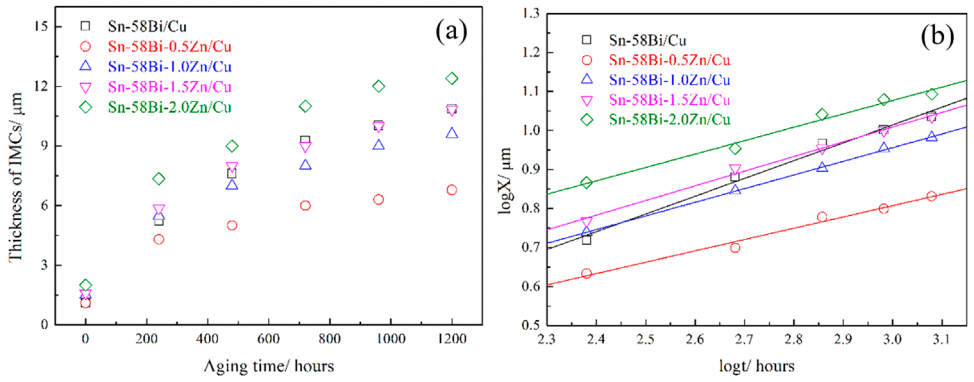

FIGURE 10
Calculation of the IMCs thickness at the Sn-58Bi-xZn/Cu interface. **(a)** Thickness vs aging time, **(b)** thickness vs aging time in logarithmic form.

TABLE 1 Time exponent and diffusion coefficient of the interfacial IMCs at 120°C.

Solder/substrate	IMCs	*n*	*D* (m^2/s)
Sn-58Bi/Cu	Cu_6Sn_5+ Cu_3Sn	0.45	5.79×10^{-20}
Sn-58Bi-0.5Zn/Cu	$Cu_6(Sn,Zn)_5$	0.29	3.66×10^{-20}
Sn-58Bi-1.0Zn/Cu	Cu_5Zn_8	0.35	6.18×10^{-20}
Sn-58Bi-1.5Zn/Cu	Cu_5Zn_8	0.37	1.03×10^{-19}
Sn-58Bi-2.0Zn/Cu	Cu_5Zn_8	0.34	1.42×10^{-19}

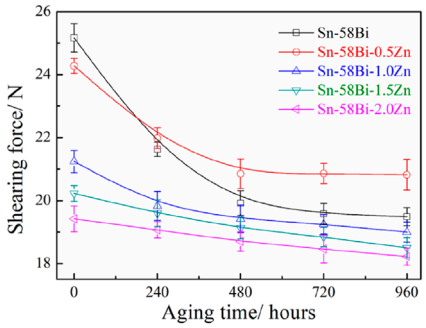

FIGURE 11
Shearing force of the composite solder joints before and after aging.

be found in the IMCs as illustrated with the red circle in Figure 6b. The as-soldered Sn-58Bi-0.5Zn/Cu was shown in Figures 6c, d. A flat layer of IMCs can be observed with the addition of 0.5 wt% Zn particles. The thickness of the IMCs layer slightly increased by comparison with the as-soldered Sn-58Bi/Cu interface. The EDS result indicated that some Sn atoms have been replaced with Zn atoms in the Cu_6Sn_5 IMCs. The composition of the IMCs changed from Cu_6Sn_5 to $Cu_6(Sn,Zn)_5$ with 0.5 wt% Zn addition. The top-view morphology of $Cu_6(Sn,Zn)_5$ is shown in Figure 6d. It can be seen that the diameter and morphology of IMCs have not been changed by minor Zn addition. Significant changes in thickness and morphology occurred when the content of Zn increased to 2.0 wt% in the Sn-58Bi solder as shown in Figures 6e, f. The thickness of IMCs at the as-soldered Sn-58Bi-2.0Zn/Cu increased with more Zn addition. It has been reported that adding about 1.7 wt% of Zn to Sn makes the γ-brass (Cu_5Zn_8) to be the first phase to form at the soldering temperature (Laurila et al., 2010). Another study found that the addition of 1 wt% Zn results in the formation of Cu_5Zn_8 IMC layer at the Sn-Bi-Zn/Cu interface (Li et al., 2006). Therefore, the composition of the IMCs in Figure 6e can be identified as Cu_5Zn_8 IMCs. The diameter of the Cu_5Zn_8 IMCs was lower than 1.0 μm which is much smaller than that of Cu_6Sn_5 and $Cu_6(Sn,Zn)_5$ IMCs. The IMCs particles changed from dense to sparse at the solder/Cu interface and may ultimately affect the mechanical properties of the solder joints as shown in Figure 6f.

Figure 7 shows the microstructure and composition of the interfacial IMCs at Sn-58Bi-xZn/Cu interface after aging at 120 °C for 40 days. Compared with the as-soldered IMCs shown in Figure 6, the thickness of the IMCs layer increased and IMCs became flattened after aging. A new interfacial IMCs layer formed at the Cu_6Sn_5/Cu interface as shown in Figure 7. According to the EDS results, the atomic percentage of Cu and Sn was approximately 3:1, indicating Cu_3Sn has formed after aging. Some voids can be found in the Cu_3Sn layer as shown in the magnified morphology in Figure 7. In the solid Sn/Cu diffusion couple, the dominant diffusion atoms are Sn and Cu in Cu_6Sn_5 and Cu_3Sn respectively (Yuan et al., 2016). The formation of Cu_3Sn can be contributed by two types of reaction. The interfacial Cu_6Sn_5 reacted with Cu to form Cu_3Sn IMCs. Meanwhile, Sn atoms diffused through the interfacial Cu_6Sn_5 IMCs and reacted with Cu to form Cu_3Sn IMCs. Due to the continuous diffusion of Cu in the Cu_3Sn, Kirkendall voids formed at the Cu_3Sn/Cu interface. Kirkendall voids are defects that will reduce the reliability of solder joints. Therefore, it is essential to inhibit the growth of Cu_3Sn IMCs.

The microstructure of the aged Sn-58Bi-0.5Zn/Cu interface is shown in Figure 7. The thickness of the IMCs is slightly lower than that of Cu_6Sn_5 IMCs at the Sn-58Bi/Cu interface. The elemental compositions of the IMCs at position P1 are shown in Figure 7d. The main components of the IMCs are Cu, Sn and contain a certain amount of Zn element. Based on the atomic percentage of element content, the IMCs can be determined as $Cu_6(Sn,Zn)_5$ compounds. It is worth noting that no compounds were generated

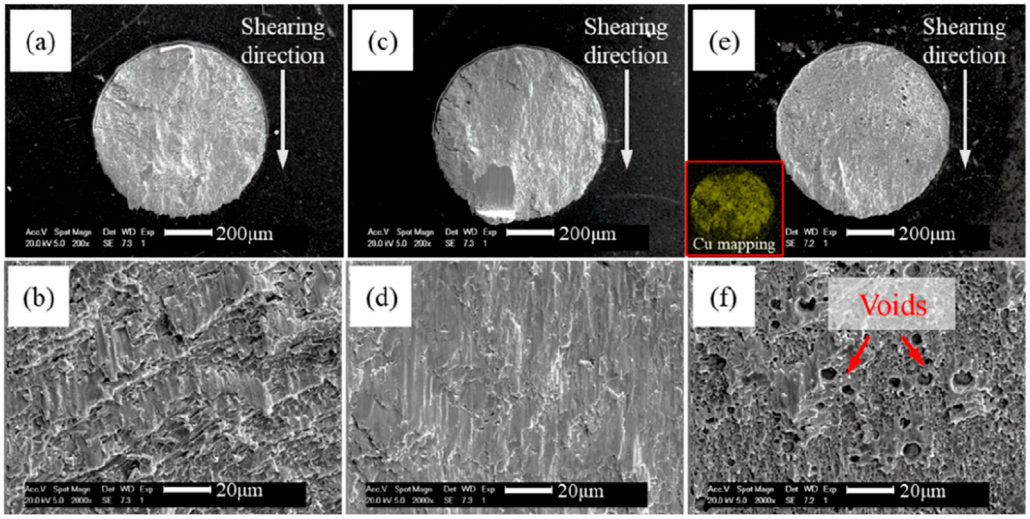

FIGURE 12
Fracture surface of the as-soldered composite solder joints. **(a, b)** Sn-58Bi, **(c, d)** Sn-58Bi-0.5Zn, **(e, f)** Sn-58Bi-2.0Zn.

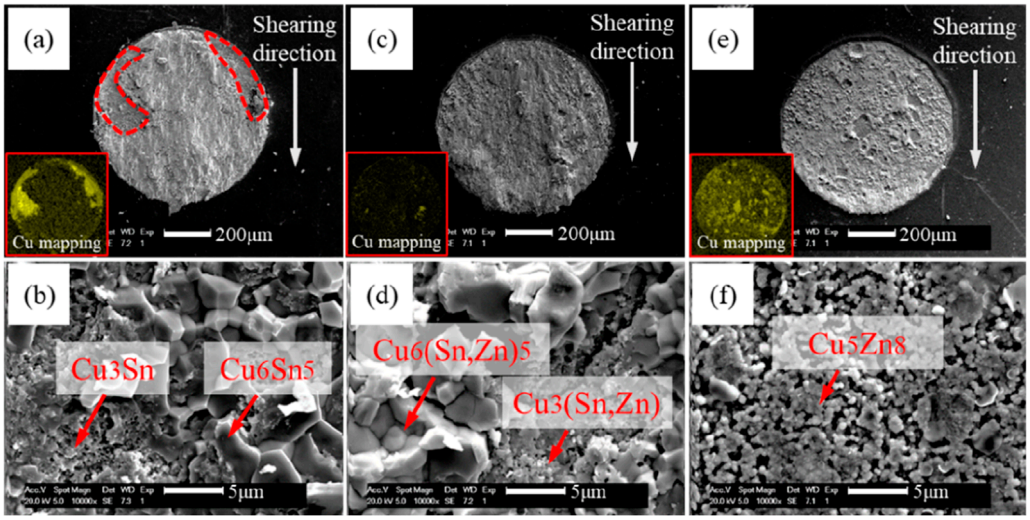

FIGURE 13
Fracture surface of the composite solder joints aged for 960 h **(a, b)** Sn-58Bi, **(c, d)** Sn-58Bi-0.5Zn and **(e, f)** Sn-58Bi-2.0Zn.

at the $Cu_6(Sn,Zn)_5$/Cu interface. This indicates that the addition of 0.5 wt% Zn in the Sn-58Bi solder delayed the growth of Cu_6Sn_5 IMCs and inhibited the generation of detrimental Cu_3Sn IMCs. With the increase of Zn content in the Sn-58Bi solder, a thick and flat IMCs layer formed at the Sn-58Bi-2.0Zn/Cu interface after aging as shown in Figure 7c. The thickness of the IMCs at the Sn-58Bi-2.0Zn/Cu interface was the thickest among the three types of solders. The elemental compositions of the IMCs at position P2 are listed in Figure 7e. The main components of the IMCs are Cu and Zn elements indicating Cu_5Zn_8 IMCs had formed after aging. By comparing the compositions of IMCs before and after aging, adding different amounts of Zn element did not change the composition of IMCs at the solder/Cu interface.

Further increasing the aging time to 50 days, the microstructure of the Sn-58Bi/Cu interface and the element mapping are shown in Figure 8. According to the distribution of Bi elements, Bi diffused through Cu_6Sn_5 and distributed in the Cu_3Sn layer. The physical properties of Bismuth are quite different from the Cu_6Sn_5 and Cu. The thermal expansion coefficient (CTE) of Bismuth decreases with the increase in temperature (Chen et al., 2024). However, the CTE of Cu_6Sn_5 and Cu increases with the increase in temperature. Therefore, the fatigue life of Sn-58Bi solder joints will reduce due to the Bi aggregation layer when bearing temperature cycling. The phenomenon occurred at the location where Cu_6Sn_5 came into contact with the Bi phase in the Sn-58Bi solder.

After aging for 50 days, the microstructure and elemental mapping of the IMCs at the Sn-58Bi-0.5Zn/Cu interface are shown in Figure 9. The IMCs near the Cu substrate showed a high content of Zn element, indicating $Cu_6(Sn,Zn)_5$ was first to generate. With the increase of aging time, the Zn near the solder/Cu interface has been consumed by the growth of IMCs. Therefore, the subsequently grown compounds at the interface were Cu_6Sn_5 IMCs. The Bi aggregation layer was not found at the interface. Meanwhile, $Cu_3(Sn,Zn)$ IMCs were hardly detected at the $Cu_6(Sn,Zn)_5$/Cu interface indicating the formation of $Cu_6(Sn,Zn)_5$ hindered the diffusion of Sn and Cu. Therefore, adding minor Zn is beneficial for the long-term reliability of Sn-58Bi solder joints.

The thickness of the interfacial IMCs at the Sn-58Bi-xZn/Cu interface was measured and plotted in Figure 10a. The thickness of the IMCs increased with the aging time. Adding 0.5 wt% and 1.0 wt% Zn into the Sn-58Bi solder decreased the growth rate of IMCs. However, further increasing the Zn content (over 1.0 wt%) will accelerate the growth of IMCs. The growth of IMCs was examined as a function of aging time. The correlation between IMCs thickness and aging time can be expressed by Arrhenius Equation 3:

$$X = X_0 + Dt^n \tag{3}$$

Where X is the average thickness of interfacial IMCs after aging, X0 is the initial average thickness of interfacial IMCs. D is the diffusion coefficient at the aging temperature, t is the aging time, n is the time exponent. Accordingly, Equation 3 can be rewritten into Equation 4:

$$\log X = n \log t + \log D \tag{4}$$

The Previous studies indicated that the value of n was determined by the atomic diffusion mechanism (Zhang and Tu, 2014). When the time exponent n is close to 1, the growth of interfacial IMCs is controlled by interfacial reaction and follows the linear law, when n is close to 0.5, the growth of interfacial IMCs is controlled by volume diffusion and follows the parabolic law, when is close to 0.33, the growth of interfacial IMCs is controlled by grain boundary diffusion and follows the parabolic law.

Figure 10b shows the thickness of interfacial IMCs as a function of aging time in log-log format. The thickness was linearly related to aging time. According to the linear fitting results, the values of n were 0.45, 0.29, 0.35, 0.37 and 0.34, respectively. The values decrease with Zn addition. Moreover, the diffusion coefficient D was calculated in this study, as listed in Table 1. The time exponent n of the IMCs grown at Sn-58Bi/Cu interface is close to 0.5 indicating the growth of IMCs is controlled by volume diffusion. After Zn was added into Sn-58Bi solder, the time exponent n was close to 0.33. It indicated that the growth of the $Cu_6(Sn,Zn)_5$ and Cu_5Zn_8 were controlled by grain boundary diffusion. The addition of Zn into the Sn-58Bi changed the atomic diffusion mechanism at the solder/Cu interface. The diffusion coefficient of the IMCs at the aging temperature of 120°C was calculated by Arrhenius Equation 3. The diffusion coefficient of the IMCs at the Sn-58Bi/Cu interface was calculated to be 5.79×10^{-20} m^2/s. The growth rate of the IMCs at the Sn-58Bi/Cu interface is much lower than that at the Sn-0.7Cu/Cu (Tian et al., 2017) and Sn-3.0Ag-0.5Cu/Cu (Tang et al., 2016) interface at 120 °C. The diffusion coefficient of $Cu_6(Sn,Zn)_5$ IMCs at the Sn-58Bi-0.5Zn/Cu interface decreased to 3.66×10^{-20} m^2/s indicating the addition of Zn inhibited the growth of IMCs. Adding more Zn into the Sn-58Bi solder changed the phase generation in the interfacial IMCs. The diffusion coefficient of Cu_5Zn_8 was slightly higher than that of Cu-Sn IMCs.

3.4 Shearing properties of Sn-58Bi-xZn solder joints

Figure 11 shows the influence of Zn content and aging time on the maximum shearing force of the composite Sn-58Bi-xZn solder joints. The Sn-58Bi joints exhibited a maximum shearing force of approximately 25.2 N before aging. The addition of Zn did not improve the shearing strength of the Sn-58Bi joints. With the increase of the Zn content, the shearing force decreases to 19.5 N when the Zn content is 2.0 wt%. The fracture surfaces of the as-solder Sn-58Bi-xZn solder joints are shown in Figure 12. Residual Sn-58Bi solder can be found on the fracture surface as shown in Figure 12a. Sn-58Bi solder has relatively low plasticity compared with Sn-Pb or other lead-free solders. The brittle fracture morphology is observed as exhibited in Figure 12b. The fracture surface of the Sn-58Bi-0.5Zn joint is shown in Figure 12c. Residual solder was observed on the fracture surface and the Cu pad was not exposed after shearing. The magnified fracture morphology of the Sn-58Bi-0.5Zn joint is shown in Figure 12d. Similar to the Sn-58Bi joint, the fracture mode was also a brittle fracture. It has been reported that the addition of Zn improved the ultimate tensile strength but decreased the ductility (Ma and Wu, 2015). In this study, the addition of 0.5 wt% Zn has a minor influence on the mechanical properties of Sn-58Bi solder joints. The fracture surface of the Sn-58Bi-2.0Zn joint is shown in Figure 12e. The fracture surface was further analyzed by EDS, the Cu elemental mapping indicating that the Cu pad was exposed after the shearing test. The fracture mode of the Sn-58Bi-2.0Zn joint is interface fracture. A plethora of voids can be observed on the surface as shown in Figure 12f. The abovementioned studies in Figure 3 indicate that the spreading rate decreases seriously when the Zn content is over 0.5 wt%. Due to the poor wettability, the soldering defects of voids were generated at the solder/Cu interface. Therefore, the shearing force decreased significantly with the excessive addition of Zn.

The shearing force of the solder joints decreased with the increase of aging time, as shown in Figure 11. After aging at 120 °C for 240 h, the shearing force of the Sn-58Bi joint decreased to 21.6 N. The shearing force of the Sn-58Bi joints ultimately stabilized at about 19.5 N after aging for 720 h. The fracture surface of the Sn-58Bi joint aged for 960 h is shown in Figures 13a, b. Interfacial IMCs of Cu_6Sn_5 and Cu_3Sn were exposed on the surface indicating the fracture mode changed from solder fracture to solder/interface mixed fracture. The shearing force of the as-soldered Sn-58Bi-0.5Zn joint decreased from 24.3N to 22.0 N after aging for 240 h. With the increase of aging time, the shearing force of the joints with 0.5 wt% Zn addition was higher than that of Sn-58Bi joints as plotted in Figure 11. The fracture surface of the Sn-58Bi-0.5Zn joint after aging for 960 h is shown in Figures 13c, d. Hardly any IMCs can be detected indicating Cu pad was not exposed on the surface. The fracture mode of the aged Sn-58Bi-0.5Zn joint was solder fracture. The location with high Cu element concentration in Figure 13c is magnified in Figure 13d. Rare amounts of $Cu_6(Sn,Zn)_5$ and $Cu_3(Sn,Zn)$ IMCs were observed.

The Sn-58Bi solder with 0.5 wt% Zn addition exhibited outstanding mechanical properties than that of pure Sn-58Bi solder. With the increase of Zn content from 1.0 wt% to 2.0 wt%, the shearing force was 21.2 N, 20.2 N and 19.4 N, respectively. Further adding Zn in the solder, the initial shearing force of joints was lower than that of Sn-58Bi. The shearing force decreased with the increase of aging time. The shearing strength of the joints with Zn content beyond 1.0 wt% was lower than the pure Sn-58Bi and Sn-58Bi-0.5Zn joints. The fracture surface of Sn-58Bi-2.0Zn aged for 960 h is shown in Figure 13e. From the uniform distribution of Cu element, it is considered that the fracture mode of the joint was interface fracture. The magnified fracture surface is shown in Figure 13f. The sparse distributed Cu_5Zn_8 IMCs particles can be observed on the surface indicating poor mechanical properties of Sn-58Bi-2.0Zn joints. The above research indicates that 0.5 wt% Zn addition into the Sn-58Bi solder is beneficial to the long-term mechanical properties. Additive more Zn is detrimental to the reliability of Sn-58Bi joints.

4 Conclusion

In this paper, micro-sized Zn particles were added into Sn-58Bi solder flux to form Sn-58Bi-xZn composite solder. The evolution of microstructure, interfacial IMCs and shearing properties during long-term aging were investigated. The conclusions are drawn as follows:

(1) Minor Zn addition had little effect on the wettability of Sn-58Bi solder. When added with the content of Zn over 0.5 wt%, the wettability significantly decreased.
(2) The addition of 0.5 wt% Zn refined the Sn-rich phase and Bi-rich phase in the Sn-58Bi solder. Neddle-like Zn phase occurred in the matrix of Sn-58Bi-2.0Zn. After aging at 120 °C for 40 days, Bi aggregated and formed bulk Bi phases due to the Ostwald ripening. The addition of Zn mitigated the aggregation and growth of Bi phases.
(3) The composition of the IMCs at the as-soldered Sn-58Bi/Cu interface was Cu_6Sn_5. With 0.5 wt% Zn addition, Cu_6Sn_5 changed to $Cu_6(Sn,Zn)_5$. Further increasing the Zn content, Cu_5Zn_8 instead of $Cu_6(Sn,Zn)_5$ generated at the Sn-58Bi-2.0Zn/Cu interface.
(4) After long-term aging, Cu_3Sn generated at the Cu_6Sn_5/Cu interface, Bi diffused into Cu_3Sn and form Bi aggregation layer. Minor Zn addition suppressed the growth of interfacial IMCs. When the Zn near the solder/Cu interface was consumed, the subsequently grown compounds at the interface were Cu_6Sn_5 IMCs. The Cu5Zn IMCs at Sn-58Bi-2.0Zn/Cu interface kept a high growth rate during aging.
(5) The Sn-58Bi-0.5Zn solder joints exhibited optimal shearing properties during aging. The cracks propagated along the solder before and after aging. The fracture mode of pure Sn-58Bi joints changed from solder fracture to solder/interface fracture after aging. When the content of Zn increased to 2.0 wt%, voids were found on the fracture surface due to the poor wettability. The fracture of Sn-58Bi-2.0Zn joints was interface fracture. The optimum amount of Zn addition to Sn-58Bi solder was 0.5 wt%.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

Author contributions

XY: Data curation, Investigation, Methodology, Writing–original draft. ST: Funding acquisition, Resources, Supervision, Writing–review and editing. MZ: Conceptualization, Formal Analysis, Validation, Writing–original draft. HJ: Validation, Writing–review and editing. JW: Formal Analysis, Writing–review and editing. BW: Data curation, Writing–review and editing.

Funding

The author(s) declare that financial support was received for the research and/or publication of this article. The National Natural Science Foundation of China (62404212). The Basic Research Program of Jiangsu (BK20230191).

Acknowledgments

The authors would like to acknowledge the National Natural Science Foundation of China (62404212) and the financial support Funded by Basic Research Program of Jiangsu (BK20230191). The authors would like to thank the Reviewers for their suggestions.

Conflict of interest

Authors XY, ST, HJ, JW, and BW were employed by Wuxi Zhongwei High-tech Electronics Co., Ltd. Authors XY, ST, HJ, JW, and BW were employed by China Key System and Integrated Circuit Co., Ltd.

The remaining author declares that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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The author(s) declare that no Generative AI was used in the creation of this manuscript.

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frontiers | Frontiers in Materials

TYPE Mini Review
PUBLISHED 15 April 2025
DOI 10.3389/fmats.2025.1584349

OPEN ACCESS

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RECEIVED 27 February 2025
ACCEPTED 03 April 2025
PUBLISHED 15 April 2025

CITATION
Lang F, Zhou Z, Liu J, Cui M and Zhang Z (2025) Review on the impact of marine environment on the reliability of electronic packaging materials.
Front. Mater. 12:1584349.
doi: 10.3389/fmats.2025.1584349

Review on the impact of marine environment on the reliability of electronic packaging materials

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Marine environments pose significant challenges to the reliability of electronic packaging materials. This review summarizes the main degradation mechanisms and reliability impacts of electronic packaging materials under marine conditions, including salt spray corrosion, high humidity, thermal cycling, and mechanical shock. Salt spray corrosion initiates localized galvanic corrosion through chloride ion (Cl^-) diffusion, creating corrosion pits and stress concentration, thereby accelerating electrochemical-mechanical coupled failures. High humidity promotes moisture ingress into polymer packaging materials, resulting in hygroscopic plasticization, weakened interfacial adhesion, and delamination failure. Thermal cycling, due to mismatched coefficients of thermal expansion (CTE), induces growth of interfacial intermetallic compound (IMC) layers at solder joints and creep-fatigue interactions, further promoting interfacial crack propagation. Mechanical shock generates transient, high-strain-rate loading, rapidly initiating and propagating cracks within brittle packaging structures, ultimately leading to structural failure. Additionally, this paper discusses the current status and limitations of Physics of Failure (PoF)-based reliability models such as the Coffin-Manson and Arrhenius models for evaluating electronic packaging reliability in marine environments. Finally, it suggests that future studies should further develop multiphysics coupling models to more accurately predict long-term material performance under extreme marine conditions.

KEYWORDS

marine environment, electronic packaging materials, salt spray corrosion, moisture-induced plasticization, temperature cycling, mechanical shock

1 Introduction

Marine environments pose severe challenges to the reliability of electronic packaging materials. Electronic systems employed in ships, ocean exploration, offshore communication, and underwater equipment frequently encounter extreme environmental factors, such as high salinity, high humidity, large temperature variations, and complex mechanical loading (Yi et al., 2015b; Jia, 2021). Generally, the internal environment of a ship remains relatively stable but not entirely uniform. During navigation, the internal temperature and humidity conditions vary depending on ship type, location, external climate, and operational status. For instance, large cruise ships typically maintain comfortable temperatures and humidity levels within passenger cabins and main public

areas to ensure comfort for passengers and crew. However, conditions can differ significantly in electronics-rich areas near the exterior or specialized compartments, such as engine rooms, control rooms, and cargo holds. These regions experience greater humidity and pronounced temperature fluctuations, placing electronic equipment under higher stress and risks. In contrast, electronic equipment on military and cargo vessels commonly faces extreme humidity levels of 85%–98% and temperature fluctuations from −40°C to 85°C. These harsh conditions represent critical challenges to the reliability of electronic packaging materials. Therefore, it is especially crucial to investigate the performance of electronic packaging materials used in these specific shipboard areas under extreme marine environmental conditions (Wang et al., 2022). Extreme environmental factors not only cause the degradation of material performance but also induce various failure modes (Comizzoli et al., 1986; Jia et al., 2020), such as metallic corrosion, solder joint fatigue, polymer insulation deterioration, and structural brittle fracture, severely affecting the stability and lifespan of electronic equipment (Zhu et al., 2008; Istrate and Mureşan, 2021). Thus, a thorough understanding of failure mechanisms of electronic materials in marine environments, and the development of reliability evaluation methodologies based on the Physics of Failure (PoF), is crucial to enhancing the long-term serviceability of electronic systems (Li et al., 2019; He et al., 2024). Specifically, salt spray corrosion is a major factor affecting the reliability of metal interconnections and solder joints in marine environments. The highly corrosive chloride ions (Cl^-) cause electrochemical corrosion in metal conductors, leading to bridging by corrosion products, short circuits, and deterioration of electrical performance. Moreover, high humidity environments accelerate moisture absorption by polymeric materials, reducing interfacial adhesion strength and exacerbating mismatches in the coefficients of thermal expansion (CTE), which promote delamination of packaging layers (Abdel-Samad et al., 2014; Deflorian et al., 2015). Under thermal cycling conditions, periodic thermal stresses arise due to CTE mismatch, inducing creep-fatigue interactions and promoting fatigue failure in solder joints. Mechanical shock generates transient, high-strain-rate loads on brittle materials and soldered structures, causing structural damage. Although numerous studies have proposed mitigation strategies for these failure mechanisms, including protective coatings, self-healing materials, and metal coatings, their durability and interfacial stability remain challenging under the combined action of salt spray, thermal cycling, and mechanical shock. Therefore, investigating the effects of marine environments on electronic packaging reliability is essential for understanding degradation mechanisms (Ding et al., 2019; Rong et al., 2021). As systematically illustrated in Figure 1, typical degradation and damage characteristics of electronic packaging materials caused by high salinity, humidity, temperature variations, and mechanical loads in marine environments are summarized.

In this review, we focus on four primary failure mechanisms impacting electronic packaging reliability in marine environments: electrochemical-mechanical coupling failures in salt spray corrosion, hygroscopic plasticization and interfacial failures under high humidity, thermomechanical fatigue damage induced by thermal cycling, and brittle fracture caused by mechanical shocks. Finally, reliability assessment approaches based on PoF models are summarized to provide theoretical support and engineering guidance for long-term stability of electronic materials used in marine environments (Neville, 1995).

2 Influence of various factors on shipboard electronic packaging materials in marine environments

2.1 Electrochemical-mechanical coupling failures induced by salt spray corrosion

The core mechanism of salt spray corrosion in marine environments involves the diffusion dynamics of chloride ions (Cl^-) within thin liquid films, which determine both the corrosion rate and morphological evolution of materials (Yi et al., 2015a). Specifically, Cl^- ions diffuse through the thin liquid film to vulnerable or defective sites on metallic surfaces, resulting in localized areas of high chloride concentration and accelerating localized pitting or galvanic corrosion. The formation of localized corrosion pits or cavities subsequently reduces the cross-sectional area of the material, causing local stress concentration and significant degradation in mechanical properties. Stress concentration induced by localized corrosion further promotes pit growth and crack initiation, resulting in a coupling effect between electrochemical corrosion and mechanical damage, ultimately leading to comprehensive material failure (Guedon-Gracia et al., 2016; Yan et al., 2016). Galvanic corrosion of Al-Cu alloys and Sn-Pb solder systems primarily manifests as accelerated anodic dissolution, whereas magnesium alloys exhibit prominent pitting corrosion behaviors influenced by alloying elements and coating structures (Grassini et al., 2011; Xiao et al., 2020). Such corrosion not only leads to yield strength degradation in Cu conductors (Zhang et al., 2014), but also causes internal delamination in magnesium alloys (Shi et al., 2013) and reduces the volume resistivity of epoxy resins, triggering insulation failure in printed circuit boards (PCBs) (Liu et al., 2022). In electronic systems, electrochemical-mechanical coupling effects often lead to multi-stage failures, including circuit shorting due to bridging by metal corrosion products (Xu et al., 2011), and corrosion channels in Ni-P coatings arising from conflicting thickness and porosity requirements (García-Rodríguez et al., 2019), all of which significantly affect the reliability of electronic packaging materials (Qin et al., 2024). Therefore, a deeper understanding of electrochemical-mechanical coupling failure mechanisms associated with salt spray corrosion in marine environments is crucial for accurately predicting the long-term performance degradation of electronic packaging materials and effectively mitigating risks to material reliability.

2.2 Hygroscopic plasticization and interfacial failure under high humidity

Under high-humidity conditions, the impact of moisture diffusion on material reliability is not confined merely to the diffusion behavior within the material but extends critically to subsequent changes in material properties and interfacial failure mechanisms. Specifically, after moisture diffuses into polymeric materials, water molecules infiltrate into the molecular

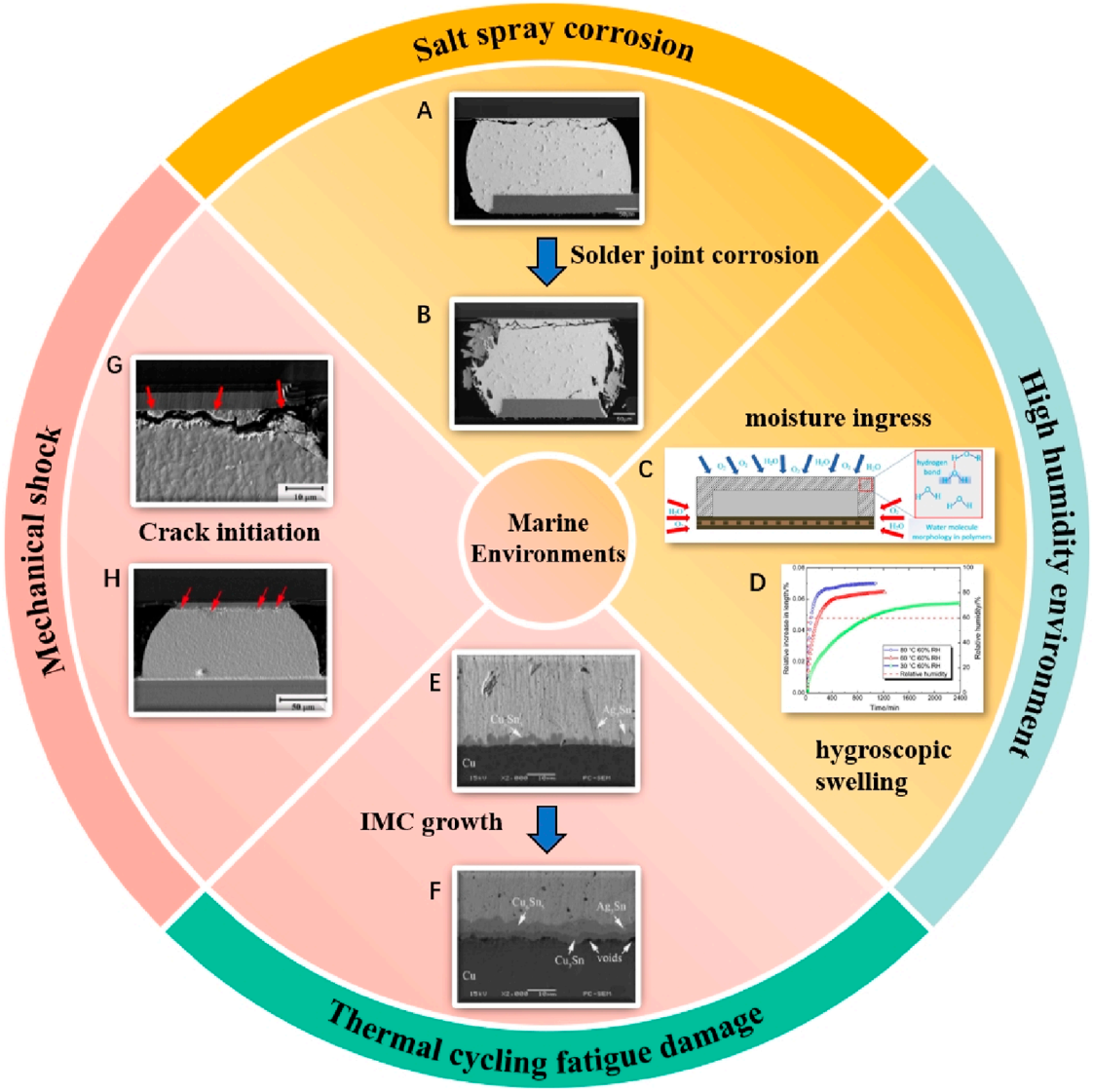

FIGURE 1
Typical degradation and damage characteristics of electronic packaging materials induced by salt spray corrosion, high humidity, thermal cycling, and mechanical shock in marine environments. (A) Cross-sectional SEM image of SAC305 solder joint after thermal cycling without salt spray pretreatment; (B) Severe corrosion of SAC305 solder joint after thermal cycling with 5% NaCl salt spray pretreatment. [Adapted from Ref (Liu et al., 2011)]; (C) Moisture ingress into packaging materials, exhibiting three states of water molecules: chemically bound water, physically adsorbed water, and free water. [Adapted from Ref (Tian et al., 2024)]; (D) Hygroscopic swelling behavior of packaging materials under different temperature and humidity conditions. [Adapted from Ref (He and Kabiri, 2022)]; (E, F) Growth of intermetallic compound (IMC) layers at solder joint interfaces and the formation of interfacial voids after aging at 150°C. [Adapted from Ref (Liu et al., 2014)]; (G, H) Crack initiation and propagation along IMC interfaces in SAC305 solder joints subjected to mechanical vibration loading, showing typical brittle interfacial fracture features. [Adapted from Ref (Pongvittayapanu et al., 2022)].

chain gaps and interact via hydrogen bonds with polymer chains. This interaction increases the mobility of polymer chain segments, causing a hygroscopic plasticization effect that significantly reduces the elastic modulus and yield strength of the polymer. The plasticization effect further reduces interfacial adhesion strength, weakening the interface's ability to resist stress (Wang et al., 2020; Zheng et al., 2022). Concurrently, moisture ingress at the interface decreases the interfacial surface free energy, impairing interfacial adhesion, and eventually causing interface delamination and layer separation (Jiang et al., 2008; Zhendong et al., 2008).

In non-hermetic environments, moisture diffusion into polymeric materials can be modeled by Fick's law, and its rate is significantly accelerated by increasing humidity and temperature. For example, moisture diffusion rates can increase by up to threefold when the ambient relative humidity exceeds 80% (Mei and Yao, 2011). Materials with higher moisture absorption capability become particularly susceptible to moisture interference in humid environments, undergoing substantial changes in material properties. Furthermore, the interactions between moisture molecules and polymeric chains alter internal stress equilibrium, introducing certain transient and complicated effects. Extensive

experimental evidence has demonstrated that moisture absorption significantly weakens the internal stress structure of epoxy resins, resulting in pronounced plasticization effects and reducing their elastic modulus by over 20% (Su et al., 2006; Nguyen et al., 2017). Moisture-induced hygroscopic expansion in printed circuit board (PCB) substrates results in mismatched coefficients of thermal expansion (CTE), increasing solder joint delamination rates under thermal cycling conditions. Experimental results indicate that delamination areas exceeding 5% in ball grid array (BGA) packages represent a failure criterion (Fan et al., 2008). It is important to note that moisture diffusion itself is not the direct cause of material failure; rather, the associated polymer plasticization and reduction in interfacial adhesion strength fundamentally drive plasticization and interfacial failures. Hygroscopic plasticization reduces structural strength, while CTE mismatch concentrates stress at interfaces, thereby accelerating delamination propagation under combined heat and humidity conditions (Tong and Ng, 2002; Shi et al., 2008).

Therefore, high humidity conditions—by inducing hygroscopic plasticization and weakening interfacial adhesion—significantly degrade the mechanical integrity and interfacial stability of electronic packaging materials, accelerating their damage progression and ultimately severely compromising their long-term reliability in marine environments.

2.3 Damage degradation induced by thermal cycling

In electronic packaging, thermo-mechanical coupling effects primarily arise from mismatches in the coefficient of thermal expansion (CTE) among constituent materials. Particularly at metal-ceramic interfaces and solder joints, these CTE mismatches cause accumulation of thermal stresses at interfaces, progressively evolving into fatigue damage during thermal cycling (Xiao et al., 2013). For SnAgCu solder joints, thermal cycling induces creep deformation at elevated temperatures, while at lower temperatures, brittle cracks tend to initiate, reflecting a creep-fatigue interaction (Nousiainen et al., 2007). Experimental studies indicate that, under cyclic conditions from −40°C to 125°C, the interfacial intermetallic compound (IMC) layer, primarily Cu_6Sn_5, progressively thickens at the solder joint interfaces, causing localized stress concentrations that subsequently reduce fatigue life (Teo, 2007). Research has demonstrated that, under typical marine environmental thermal cycling conditions (−40°C–125°C at approximately 12 cycles/hour), IMC layers initially grow rapidly, then gradually stabilize, following a characteristic parabolic growth pattern involving a rapid initial growth phase, a stable growth phase, and eventually a coarsening phase. With increasing numbers of thermal cycles, the interfacial IMC layers transition from dense structures to porous and coarsened morphologies, accompanied by void formation and micro-crack initiation. These changes significantly degrade the mechanical performance of the solder joint interface and dramatically increase the probability of interfacial failure beyond a critical number of cycles (Xu et al., 2021; Zhou et al., 2022). Furthermore, the recrystallization of solder joints is identified as a key mechanism for crack propagation (Schmitz et al., 2014). Under thermal cycling, significant degradation in mechanical properties and reliability of packaging materials occurs. For instance, aluminum alloy heat sinks experience a reduction in yield strength with increasing cycles, while plastic encapsulation materials undergo glass-transition processes at elevated temperatures, becoming more brittle at lower temperatures (Khatibi et al., 2018). In solder joint failures, cracks commonly propagate along Cu_6Sn_5/SnAgCu interfaces in ball grid array (BGA) packages, with failure rates significantly elevated under high cyclic loading conditions (Chen et al., 2013). Additionally, substrate warpage may trigger component debonding, particularly in packaging structures with substantial CTE mismatches (Xie et al., 2009). Thus, fatigue damage driven by thermo-mechanical coupling effects under thermal cycling conditions significantly accelerates performance degradation and interfacial failure risks of electronic packaging materials, critically affecting their long-term reliability and service life in marine environments.

2.4 Dynamic loading and brittle fracture caused by mechanical shock

In marine environments, dynamic loading induced by mechanical shock typically manifests as transient shock waves characterized by high strain rates. When shock waves impact electronic packaging structures, initial transmission and reflection occur at the outer structural interfaces. The superposition of reflected and incident waves significantly amplifies localized stresses within the packaging (Gharaibeh, 2022). Specifically, as shock waves propagate through multilayered structures such as chips, solder joints, substrates, and encapsulants, partial reflections and transmissions arise due to differences in mechanical impedance between distinct materials. The resulting wave interference markedly increases transient stress amplitudes, particularly at structurally vulnerable regions including chip-solder interfaces, package corners, and pin roots, where stresses can be several times higher than elsewhere. Consequently, this effect rapidly initiates and propagates micro-cracks within solder interfaces or brittle materials, ultimately culminating in evident brittle failure (Liu et al., 2021; Wu and Chang, 2021).

Experimental studies (Zhou et al., 2023) indicate that stress concentrations caused by propagating shock waves, especially at metal-ceramic or metal-polymer interfaces, readily induce localized failures, resulting in solder joint detachment or chip-substrate interface cracking. Numerical simulation results (Jiang et al., 2024) further reveal that increasing shock loads accelerate interfacial micro-crack propagation, causing fatigue-induced solder joint fractures and compromising overall system reliability. In practical marine applications, such rapid failures, particularly under frequent shock loading, may lead to immediate or cumulative equipment failure, severely impacting the operational stability of marine electronic systems. Moreover, material responses to shock loading vary significantly, with brittle materials showing pronounced reductions in strength and toughness under high-strain-rate conditions (Zheng et al., 2017). Studies demonstrate rapid initiation and propagation of internal micro-cracks in metallic materials (e.g., SAC305 solder balls), culminating in brittle fracture under shock conditions (Jenq et al., 2009; Long et al., 2020). Dynamic responses of materials encompass critical mechanisms such as crack

initiation sites, propagation paths, and fracture modes (Gross and Seelig, 2011). Failure mechanisms in specific structural components also involve plastic deformation of connector pins, predominantly influenced by gold-plating thickness; insufficient plating thickness can result in permanent bending of copper substrates under shock, causing electrical connection failure (Ling et al., 2019). Furthermore, stress concentrations at package corners render chip encapsulation particularly susceptible to fracture during mechanical shock events (Lu et al., 2012). Consequently, the stress concentration effects induced by mechanical shocks significantly accelerate crack initiation and propagation within electronic packaging interfaces, leading directly to brittle structural failure. This damage mechanism severely compromises the long-term reliability and operational stability of electronic packaging materials in marine environments (Gao and Oterkus, 2018; Hu et al., 2022).

3 Reliability impacts on shipboard electronic packaging materials in marine environments

In marine environments, the reliability of electronic packaging materials is simultaneously affected by multiple factors, including salt-spray corrosion, high humidity, thermal cycling, and mechanical shock. To quantitatively assess these impacts, Physics-of-Failure (PoF) based approaches are employed to analyze material reliability under various environmental stresses. The following section introduces physical models tailored to different failure mechanisms and discusses their applicability within marine conditions.

High humidity and salt spray in marine environments accelerate the degradation of electronic devices, adversely affecting gate oxide layers, metal interconnects, solder joints, and packaging materials. High humidity alters the charge distribution within oxide layers, accelerating Time-Dependent Dielectric Breakdown (TDDB), while ionic contamination from salt spray decreases dielectric insulation, prompting premature failures. Furthermore, temperature fluctuations exacerbate Hot Carrier Injection (HCI), intensifying device deterioration. Metal interconnects and solder joints are particularly susceptible to electromigration (EM) and corrosion; salt-spray corrosion reduces metallic stability, and elevated humidity accelerates ionic migration, aggravating electromigration-induced failures that eventually lead to interconnect fractures. Thermal fatigue failures in solder joints and packaging materials can be modeled using Coffin-Manson, Norris-Landzberg, and Arrhenius models, as high humidity combined with temperature cycling intensifies expansion mismatches and elevates failure risks. Additionally, mechanical shocks induce crack propagation, often analyzed by the Paris Law model, while salt spray exacerbates interfacial cracking, and humid conditions soften packaging materials, reducing their mechanical strength and accelerating failure. Table 1 summarizes these failure-physics models widely used for reliability assessment and accelerated test design to predict the service life of electronic packaging devices in marine environments.

To enhance reliability under marine conditions, significant progress has been achieved through material modifications targeting extreme humidity, salinity, and temperature fluctuations. For instance, polymers with low moisture absorption, such as modified epoxy resins, have demonstrated significantly reduced hygroscopic plasticization in experiments, thus improving the stability and long-term reliability of electronic packaging materials (Bone et al., 2022; He and Kabiri, 2022). Additionally, novel corrosion-resistant metal alloys have increasingly been utilized in marine electronic systems due to their enhanced resistance to galvanic corrosion, effectively reducing corrosion-related failures in metallic components (Adesina et al., 2021). Beyond these material modifications, researchers have explored various advanced coatings, including nano-coatings and self-healing coatings, aimed at improving corrosion resistance in packaging materials and extending their service lifetimes. Surface modifications enabled by nanotechnology have provided superior protection by effectively blocking moisture and ionic ingress, slowing corrosion processes (Son et al., 2023). Moreover, modified ceramic materials have demonstrated exceptional stability under high-temperature and corrosive conditions, particularly suitable for marine applications demanding extremely high reliability (Yang et al., 2022).

It is noteworthy that currently there are no standards or guidelines specifically dedicated to electronic packaging materials used in marine environments. Although some existing standards, such as ISO 9227 and ASTM B117, provide cyclic salt-spray test methods capable of simulating marine salt-spray corrosion, they lack specific regulations addressing the reliability of electronic equipment operating under marine conditions. Standards like IPC-SM-785 provide accelerated reliability testing procedures for PCBs and related electronic interconnect products, and JEP122H addresses failure mechanisms and modeling for semiconductor devices under accelerated testing conditions. However, while these standards effectively simulate extreme temperature and humidity conditions, they do not directly address the unique demands posed by marine environments. The specificity of marine conditions—including high salinity, elevated humidity, temperature fluctuations, and mechanical shock—necessitates the establishment of specialized standards and guidelines tailored explicitly for electronic packaging materials in marine applications. Consequently, focused research on reliability assessment methods and testing procedures for electronic packaging materials under marine conditions is critically important for filling this standards gap.

In conclusion, factors such as high humidity, salt-spray corrosion, temperature cycling, and mechanical shock significantly affect the reliability of electronic packaging materials in marine environments. The application of PoF models enables quantitative evaluation of these environmental stresses, facilitating accurate predictions of device service lifetimes in marine conditions. To address these reliability challenges, researchers have notably enhanced material stability and durability through modifications such as low moisture-absorption polymers, corrosion-resistant metal alloys, and advanced coating materials. However, current standards and guidelines predominantly focus on terrestrial conditions, leaving a critical need for the development of specialized marine-environment standards and reliability assessment methods. Thus, establishing such standards will significantly contribute to improving the long-term stability and reliability of electronic systems deployed in marine environments.

TABLE 1 Failure mechanisms and models in semiconductor devices.

Failure mechanism	Failure mechanism models	Ref.
HCI	$TTF = A_h(I_{sub})^{-N_h}\exp(E_{ah}/kT)$	Chang et al. (2010)
TDDB	$TTF = A_t\exp(-a_tE_{ox}/kT)\exp(E_{at}/kT)$	Crook (1979), Anolick and Nelson (2009)
EM	$TTF = A_e(J-J_{crit})^{-N_e}\exp(E_{ae}/kT)$	Black (1969), De Orio et al. (2010)
NBTI	$TTF = \left[\frac{\Delta p_t}{A_0}\cdot\exp\left(\frac{E_{aa}}{kT_{app}}\right)\cdot\left(V_{G,appl}\right)^{\alpha}\right]^{\frac{1}{n}}$	Rabiei et al. (2018)
Corrosion	$TTF = A_c\exp(-a_cRH)\exp(E_{ac}/kT)$	Rongen et al. (2014)
Thermal Fatigue	$N_f = C(\Delta\varepsilon)^{-m}$	Darveaux (2002)
Solder Joint Fatigue	$N_f = A(\Delta T)^{-m}\exp(E_{an}/kT)$	Lall et al. (2011)
Temperature-Dependent Failure	$TTF = A\exp(E_{aa}/kT)$	Hartler (1987)
Crack Propagation	$\frac{da}{dN} = C(\Delta K)^m$	Xu et al. (2012)

4 Conclusion

This paper systematically reviews the primary failure mechanisms and reliability implications of extreme environmental factors—such as salt-spray corrosion, high humidity, thermal cycling, and mechanical shock—on electronic packaging materials in marine environments. Research indicates that salt-spray corrosion initiates localized galvanic corrosion through Cl^- ion penetration, creating internal corrosion pits and stress concentrations that trigger pronounced electrochemical-mechanical coupling failures. High humidity induces moisture-induced plasticization within packaging materials, significantly weakening interface strength and causing interfacial delamination failures. Under thermal cycling, mismatches in coefficients of thermal expansion (CTE) accelerate interfacial IMC layer growth and induce creep-fatigue damage in solder joints, deteriorating interface reliability. Mechanical shock loading notably exacerbates brittle interface crack initiation and rapid propagation, leading to structural failure. Although current Physics-of-Failure (PoF)-based reliability models can partly describe and predict the degradation behavior under single environmental factors, the complexity arising from multi-factor coupling in marine environments limits their comprehensive accuracy for evaluating long-term material service performance. Therefore, it is critically necessary to establish and develop more precise multi-physics coupled models that integrate material degradation behaviors and damage mechanisms, as well as specialized reliability standards and assessment methodologies tailored specifically to marine environments, to improve the long-term stability and reliability of electronic packaging materials in extreme marine conditions.

Author contributions

FL: Writing – review and editing. ZeZ: Investigation, Writing – original draft, Writing – review and editing. JL: Methodology, Supervision, Writing – review and editing. MC: Methodology, Writing – review and editing. ZoZ: Conceptualization, Supervision, Writing – review and editing.

Funding

The author(s) declare that financial support was received for the research and/or publication of this article. This work was supported by the Qin Chuang Yuan high-level innovation and entrepreneurship talent project (No. QCYRCXM-2022-306), and the Natural Science Foundation of Chongqing (No. CSTB2022NSCQ-MSX0574).

Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Generative AI statement

The authors declare that no Generative AI was used in the creation of this manuscript.

Publisher's note

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frontiers | Frontiers in Materials

TYPE Mini Review
PUBLISHED 24 April 2025
DOI 10.3389/fmats.2025.1582990

OPEN ACCESS

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RECEIVED 25 February 2025
ACCEPTED 19 March 2025
PUBLISHED 24 April 2025

CITATION
Xue Y, Li R, Deng Y, Zhang Z, Chen J, Ma A and Wen R (2025) Research progress in interface optimization and preparation technology of high thermal conductivity diamond/copper composite materials. *Front. Mater.* 12:1582990. doi: 10.3389/fmats.2025.1582990

Research progress in interface optimization and preparation technology of high thermal conductivity diamond/copper composite materials

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With the miniaturization and integration of microelectronic components, the demand for high-thermal-conductivity electronic packaging materials has grown substantially. Diamond/copper (Dia/Cu) composites have become a focus of research due to their ultra-high thermal conductivity and low coefficient of thermal expansion. However, poor interfacial bonding and high interfacial thermal resistance between diamond and copper limit their practical performance. This paper reviews strategies to enhance interfacial bonding, including diamond surface metallization (e.g., electroless plating, magnetron sputtering, molten salt method, vacuum electroplating, and embedding) and copper matrix alloying (e.g., gas atomization and alloy smelting), and evaluates their effects on thermal transport properties. Additionally, the influence of preparation processes—such as vacuum hot-pressing sintering, high-temperature high-pressure sintering, spark plasma sintering, and melt infiltration on the microstructure and thermal conductivity of composites are discussed. Key factors including diamond surface roughness, particle size, volume fraction, and sintering conditions (e.g., temperature, pressure, and dwell time) are analyzed. Experimental and computational studies demonstrate that systematic optimization of these factors enhances the thermal conductivity of Dia/Cu composites, providing critical insights for developing next-generation high-performance electronic packaging materials.

KEYWORDS

high thermal conductivity, diamond/copper, composite material, surface metallization, matrix alloying

1 Introduction

The relentless advancement of high-power density and miniaturization in modern microelectronics has positioned thermal management as the paramount challenge for ensuring device reliability (Wu et al., 2024; Moore and Shi, 2014; Jiang et al., 2015). To mitigate this thermal bottleneck, substantial research efforts have been directed toward developing advanced electronic packaging materials with superior thermal transport capabilities. Contemporary packaging materials are systematically classified into three

distinct categories based on composition: ceramic-based, polymer-based, and metal-based systems. While ceramic (AlN: 170–320 W m^{-1}·K^{-1}) and polymer (epoxy: 0.2 W m^{-1}·K^{-1}) systems face inherent thermal limitations, copper matrix composites—particularly diamond-reinforced variants—offer superior solutions (Li et al., 2022a; Gu et al., 2016; Dai et al., 2020).

Diamond/copper composites integrate the extreme anisotropic thermal conductivity (1,200–2,000 W m^{-1}·K^{-1}) and ultralow CTE (≈1 × 10^{-6} K^{-1}) with copper's processability (400 W m^{-1}·K^{-1}) (Ward et al., 2009; Dai et al., 2020). However, interfacial thermal resistance (TBR >10^{-7} m^2 K·W^{-1}) caused by weak metal-ceramic bonding degrades performance via phonon scattering. Current efforts focus on interfacial engineering strategies, including diamond surface metallization and matrix alloying, to minimize TBR and optimize thermal transport (Zhang et al., 2018; Dai et al., 2020).

The relentless advancement of high-power-density microelectronics demands packaging materials capable of dissipating heat fluxes exceeding 1 kW/cm^2 to ensure device reliability. While ceramics (AlN: 170–320 W m^{-1}·K^{-1}) and polymers (epoxy: <0.2 W m^{-1}·K^{-1}) systems are thermally inadequate, diamond/copper (Dia/Cu) composites offer unmatched potential by synergizing diamond's anisotropic thermal conductivity (1,200–2,000 W m^{-1}·K^{-1}) and ultralow CTE (≈1 × 10^{-6} K^{-1}) with copper's processability (400 W m^{-1}·K^{-1}; Cui et al., 2024; Dai et al., 2020). However, interfacial thermal resistance (TBR >10^{-7} m^2 K·W^{-1}) arising from weak diamond-Cu bonding remains a critical bottleneck, degrading thermal transport via phonon scattering. Recent studies emphasize interfacial engineering—such as surface metallization (e.g., W, TiC coatings) and matrix alloying (e.g., Zr, B)—to mitigate TBR. Yet, the scalable fabrication of defect-free carbide layers and precise control of interfacial crystallography for phonon matching remain unresolved (Li R. et al., 2022). This work addresses these gaps by systematically optimizing metallization parameters and alloy compositions to achieve TBR <5 × 10^{-8} m^2 K·W^{-1}, bridging the divide between lab-scale innovation and industrial viability.

2 Diamond surface metallization

Diamond surface metallization involves depositing carbide-forming elements (e.g., W, Mo, Cr, Ti) through various coating techniques to create a continuous carbide interlayer (Zhang et al., 2023). In unmodified diamond/copper composites, pristine diamond surfaces exhibit poor interfacial adhesion The copper matrix forms weakly bonded interfaces, exhibiting excessive thermal boundary resistance (TBR > 10^{-7} m^2 K·W^{-1}) that severely degrade thermal conductivity (typically <400 W m^{-1}·K^{-1}).The metallized carbide layer addresses these limitations through three mechanisms: (i) enhancing interfacial bonding strength via chemical interactions, (ii) reducing porosity-induced thermal resistance through conformal coating, and (iii) protecting diamond from graphitization during processing. Established metallization methods include electroless plating, magnetron sputtering, molten salt synthesis, vacuum electroplating, and embedded powder sintering (Zhou et al., 2023).

2.1 Electroless Plating (ELP)

Electroless plating, also known as chemical plating or autocatalytic plating, is a metal deposition method that reduces metal ions in a plating solution to metallic form and deposits them onto substrate surfaces through the action of appropriate reducing agents, without the application of external electrical current. Typically, the surface of the substrate to be plated requires pretreatment, particularly for non-conductive and hydrophobic materials such as diamond. Li et al. (2022b) formed a thin TiC coating on diamonds using molten salt with NaCl-KCl-NaF, then applied electroless plating of Cu. The hot-pressing diamond/Cu composite with 60 vol% modified diamonds exhibits the best thermal conductivity of 495.5 W·m^{-1} K^{-1}. However, ELP has limited industrial adoption due to three critical drawbacks. First, ELP relies on physical metal attachment rather than atomic diffusion bonding, leading to poor coating-substrate adhesion (interfacial strength <50 MPa). Second, the deposited metallic layer may catalyze the graphitization of diamond at elevated temperatures, significantly degrading its intrinsic thermal conductivity. Third, the non-uniform nucleation and growth characteristics of electroless plating often lead to incomplete surface coverage, particularly on geometrically complex substrates (Liu L.-Y. et al., 2023).

2.2 Magnetron sputtering

Magnetron sputtering utilizes an electric field to generate a plasma discharge in a low-pressure argon environment. Electrons accelerated by the field ionize argon atoms, producing argon ions and secondary electrons. The ions are then accelerated toward the cathode (target material), where their bombardment sputters target atoms via momentum transfer, forming the coating layer. The sputtered atoms and secondary electrons migrate to deposit on diamond surfaces, forming uniform coatings. Sang et al. (2021) employed this technique to deposit tungsten coatings (45–300 nm thickness) on diamond particles, followed by pressureless infiltration of liquid copper into the coated diamond bed to fabricate diamond/copper composites. Characterization revealed that tungsten coatings exceeding 93 nm thickness demonstrated optimal effectiveness in enhancing composite densification and reducing interfacial thermal resistance between diamond reinforcements and the copper matrix (Zhao et al., 2021).

2.3 Molten salt coating (MSC)

Molten salt coating involves a diffusion-driven metallurgical reaction where modified metal powders are dissolved in chloride-based salt baths. At elevated temperatures (typically 600°C–900°C), diamond particles react with molten metallic species over 1–2 h to form chemically bonded carbide interfacial layers. Li et al. (2022b) systematically investigated chromium carbide formation on diamond surfaces by introducing NaF into a ternary NaCl-KCl-LiCl molten salt system within 600°C–750°C. Their experimental investigations demonstrated that NaF served as an effective activator, enabling the formation of Cr_7C_3 coatings at temperatures below 697°C through enhanced ion mobility. In a separate study, Kang et al. (2013b)

synthesized molybdenum carbide (Mo_2C)-coated diamond particles via MSC, followed by vacuum pressure infiltration to fabricate copper-diamond composites. Microstructural characterization revealed that the Mo_2C interlayer significantly improved wettability between diamond reinforcements and copper matrix. The composite containing 65 vol% Mo_2C -coated diamond exhibited exceptional thermal conductivity of 608 W m^{-1}·K^{-1}, representing a 142% enhancement compared to uncoated diamond counterparts.

2.4 Vacuum micro-evaporation plating (VMEP)

Vacuum micro-evaporation plating (VMEP) enables low-temperature (<500°C) synthesis of interfacial compounds through activated metal-diamond reactions under vacuum, offering cost-effective processing with minimal structural damage. Wu et al. demonstrated that VMEP-processed Cu/diamond composites achieve thermal conductivities up to 846.5 W m^{-1}·K^{-1} when employing large diamond particles (400 μm diameter) (Wu et al., 2019). This enhancement arises from optimized interfacial bonding that facilitates coherent phonon transport, with conductivity scaling proportionally to particle size due to reduced interfacial defect density. However, its application in precision thermal management components is constrained by high equipment costs, limited geometric adaptability, and diamond degradation risks under prolonged high-pressure sintering. Addressing these limitations requires prioritized development of low-temperature activating agents and pulsed pressure strategies to optimize interfacial engineering while mitigating mechanical/thermal damage.

2.5 Powder encapsulation and sintering (PES)

PES employs solid-state carbon-metal interdiffusion at 900°C–1,200°C to create adherent carbide interfacial layers. To further optimize interfacial properties, Li et al. achieved 670 W m^{-1}·K^{-1} in Cu-WC composites through W_2C/WC graded interfaces formed at 1,050°C (Li et al., 2015). Similarly, Shen et al. enhanced this to 726 W m^{-1}·K^{-1} via MoC interlayers using pressure-assisted melt infiltration (Shen et al., 2012). The nanostructured carbide interfacial layers in these studies effectively suppress interfacial phonon scattering by establishing coherent crystallographic continuity with the matrix phase. However, PES faces three limitations: (1) Diamond graphitization (>900°C) degrading thermal properties; (2) Thermal stress-induced delamination (ΔT >800°C) in large components; (3) Stoichiometric heterogeneity in carbide phases (e.g., Cr_3C_2/Cr_7C_3 mixtures from EBSD). Mitigation strategies include thermal gradient optimization and precursor particle size control for scalability.

3 Matrix alloying

Matrix alloying represents a widely implemented interface engineering strategy for copper-based diamond composites. This non-destructive processing approach involves pre-introduction of strategic alloying elements (e.g., Zr, B, Cr) into the copper matrix prior to composite fabrication. During thermal processing, these active elements diffuse toward diamond-copper interfaces, reacting with surface carbon atoms to form epitaxial carbide transition layers. Such interfacial engineering simultaneously optimizes phonon transport pathways through crystallographic matching and enhances interfacial bonding strength, ultimately elevating the composite's thermal conductivity (Liu et al., 2020).

3.1 Gas atomization

Gas atomization enables the synthesis of Cu-Zr alloy powders (0.25–1.0 wt% Zr) through high-velocity inert gas fragmentation of molten metal streams (Zhu et al., 2022). Chu et al. demonstrated that hot-press sintering of gas-atomized Cu-Zr with diamond yields composites where Zr content critically governs interfacial carbide evolution (Chu et al., 2013). At 0.5 wt% Zr, discontinuous ZrCx nanostructures (two to five nm thick) form at diamond-Cu interfaces, optimizing phonon transmission to achieve 615 W m^{-1}·K^{-1} thermal conductivity. Excessive Zr (1.0 wt%) promotes continuous ZrCx interphases (15–20 nm thick), introducing phonon scattering at ZrCx/Cu boundaries that elevate interfacial thermal resistance (Chu et al., 2013). This nanoscale control of carbide discontinuity highlights the precision required in alloy design for thermal management applications.

3.2 Alloy smelting process

Alloy smelting enables precise interfacial engineering through thermochemical synthesis of modified Cu matrices. Weber et al. demonstrated Cr-B co-alloying via pressurized melt infiltration creates metastable CrBx interfacial phases, achieving 600 W m^{-1}·K^{-1} at 60 vol% diamond loading (Weber and Tavangar, 2007). Bai et al. further optimized this strategy, showing 0.3 wt% B addition precipitates discrete CrB2 nanostructures (three to eight nm) at interfaces, yielding 868 W m^{-1}·K^{-1} – a 44.7% enhancement over unmodified systems (Bai et al., 2018).

Critical analysis reveals carbide interlayers require dual optimization: (1) intrinsic thermal conductivity >400 W m^{-1}·K^{-1} and (2) thickness control (50–100 nm). Sub-30 nm layers inadequately relieve lattice mismatch stresses, while >150 nm interphases induce phonon scattering at grain boundaries. Ciupiński et al. validated this through Cu-0.65Cr composites with 81 ± 5 nm Cr3C2 layers, achieving 687 W m^{-1}·K^{-1} (92% of Hashin-Shtrikman theoretical limit) via gradient thermal protocols (Ciupiński et al., 2017). These findings establish atomic-scale interface tailoring as paramount for maximizing thermal transport in electronic packaging materials (Zhong et al., 2024).

4 Optimization of fabrication processes for diamond/copper composites

The selection of fabrication methodology critically governs the microstructure development, relative density (>98% theoretical), and interfacial integrity of diamond/copper composites, making

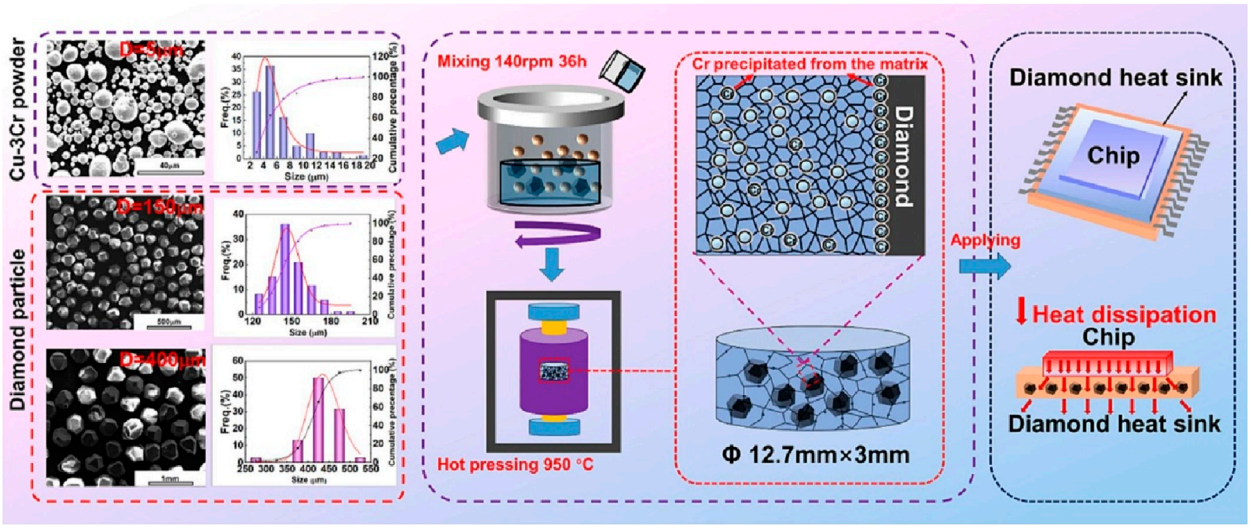

FIGURE 1
The sketch of the preparation process and the application of composites (Zhang and Lei, 2024).

process optimization essential for achieving superior thermal conductivity. Established consolidation techniques include vacuum hot-press sintering, high-pressure high-temperature (HPHT) sintering, spark plasma sintering (SPS), and melt infiltration, each with distinct interfacial engineering mechanisms. A typical sketch of the preparation process of composites is shown in Figure 1.

4.1 Vacuum hot-press sintering

Vacuum hot-press sintering integrates thermal activation and uniaxial pressure (typically 20–100 MPa) within vacuum chambers ($<10^{-3}$Pa) to consolidate diamond-copper powder mixtures. The applied pressure facilitates particle rearrangement and plastic deformation, enhancing interfacial bonding through solid-state diffusion. This synergistic effect enables composites with near-theoretical density and optimized thermal pathways (Tan et al., 2020; Liu X. et al., 2023; Zhang et al., 2024).

Shen et al. (2010) fabricated diamond/Cu-5wt%Si composites via low-pressure sintering (25.5 MPa) at 1,000°C for 10 min, achieving a thermal conductivity of 455 W m^{-1}·K^{-1}. Advanced interfacial engineering was demonstrated by Zhang et al. (2015), who employed tungsten-coated diamond particles with electroless copper overlayers. Subsequent consolidation at 900°C under 80 MPa for 30 min yielded composites with 721 W m^{-1}·K^{-1} thermal conductivity, attributable to the graded W-Cu interfacial architecture.

4.2 High-temperature high-pressure (HPHT) sintering

HPHT sintering leverages extreme conditions (three to six GPa, 1,000°C–1,300°C) to induce atomic-scale dissolution-reprecipitation mechanisms between diamond and copper matrix (Hayat et al., 2022). This process achieves metastable phase equilibria through: (1)Diamond surface graphitization inhibition via pressure-stabilized sp^3bonding; (2)Liquid-phase enhanced copper diffusion along diamond grain boundaries; (3)Stress-assisted recrystallization for void elimination (Chen et al., 2013).

Yoshida and Morigami (2004) synthesized 70 vol% diamond/Cu composites using 90–110 μm diamonds under 4.5 GPa at 1,200°C, achieving a record thermal conductivity of 742 W m^{-1}·K^{-1}. While HPHT enables ultra-dense composites (>99.5% density), its practical implementation faces challenges including technically demanding equipment specifications (multi-anvil hydraulic systems) and prohibitive operational costs for large-scale production.

4.3 Spark plasma sintering (SPS)

SPS employs pulsed direct currents (1,000–5000 A) and uniaxial pressures (30–100 MPa) to achieve rapid densification (≤500°C/min) via joule heating and electron bombardment-activated surface diffusion (Liu et al., 2019). While enabling near-full densification, SPS-fabricated composites exhibit inherent constraints: interfacial porosity (5–15 vol%) and limited component dimensions (<50 mm diameter), restricting thermal conductivity optimization. Liu et al. demonstrated SPS-processed 50 vol% diamond/Cu composites achieve exceptional high-temperature tribological performance (friction coefficient: 0.133; wear rate: 2.1–2.7 × 10^{-6} mm^3/Nm at 500°C), attributed to *in situ* formation of CuO lubricants from oxidized debris. Pan et al. enhanced thermal transport by integrating ZrC/Zr bilayer coatings via SPS, attaining 609 W m^{-1}·K^{-1} at 60 vol% loading through controlled zirconium-carbon reactions (Pan et al., 2019). These advances highlight SPS's dual capability in tailoring interfacial chemistry and rapid prototyping, though scalability remains hindered by residual porosity and dimensional limitations (TAO et al., 2014).

4.4 Melt infiltration technique

Beyond the aforementioned consolidation techniques, emerging methodologies such as chemical vapor deposition (CVD) and cold-press sintering demonstrate niche potential for fabricating diamond/copper composites. To achieve next-generation thermal management materials ($\kappa > 900$ W m^{-1}·K^{-1}), researchers should focus on synergistic optimization.Melt infiltration leverages capillary forces and external pressure (1–15 MPa) to drive molten metal through diamond beds, with infiltration kinetics governed by pressure-particle size synergies. Increased pressure enhances flow velocity, while larger diamond particles (>500 μm) reduce capillary resistance through widened interstices, promoting coherent Cu-diamond interfaces (Dai et al., 2020). Kang et al. achieved 680.3 W m^{-1}·K^{-1} in Cu-B/diamond composites via 10 MPa infiltration, where continuous B4C layers optimized interfacial bonding (Kang et al., 2013a). Bai et al. elevated this to 868 W m^{-1}·K^{-1} through B-alloyed matrices, while Dai et al. (Bai et al., 2018) demonstrated record 930 W m^{-1}·K^{-1} conductivity in Cu-0.5Zr composites via ZrC-induced acoustic impedance matching (Dai et al., 2020). Acoustic impedance matching uses intermediate layers (e.g., ZrC) to reduce phonon reflection by bridging impedance gaps between matrix and reinforcement, enhancing thermal conductivity. These breakthroughs underscore the criticality of carbide-mediated interface engineering in balancing infiltration dynamics and phonon transport efficiency. Future advances demand synergistic optimization of alloy chemistry and pressure-temperature protocols to surpass 900 W m^{-1}·K^{-1} thresholds for next-gen thermal management.

5 Critical performance Determinants

5.1 Diamond surface roughness

Compared to smooth diamond surfaces, roughened diamond surfaces increase the contact area with modifying elements, thereby promoting carbide nucleation and enhancing the thermal performance of diamond/copper composites. Merabia and Termentzidis (2014) employed molecular dynamics simulations to study interfacial roughness effects on thermal boundary conductance (TBC) in solid-solid systems (Merabia and Termentzidis, 2014). They found TBC remains constant at low roughness (approaching flat interface values), but exceeds planar interface levels under significant roughness, demonstrating boundary-dominated heat transfer mechanisms. Wu et al. (2019) demonstrated a thermal conductivity improvement of 45% (685 W m^{-1}·K^{-1}) in modified diamond/copper composites by surface roughening via molten potassium nitrate treatment. This enhancement was attributed to optimized interfacial interactions resulting from the increased surface roughness.

5.2 Diamond particle size and volume fraction

The thermal conductivity of diamond/copper composites is governed by percolative networks formed by diamond particles, with their size and volume fraction critically dictating phonon transport efficiency. At low volumetric loadings (<35 vol%), uniform dispersion creates excessive interparticle distances that impede phonon-mediated heat transfer (Monje et al., 2014). Increasing diamond content to 60–70 vol% establishes low-thermal-resistance percolation pathways, yet exceeding 70 vol% induces defect proliferation through incomplete copper infiltration, generating interfacial voids and cracks that dominate phonon scattering. This dual-phase behavior results in a characteristic thermal conductivity maximum at critical diamond loading. Surface modification (e.g., carbide coatings) elevates this threshold by enhancing interfacial phonon coupling, as demonstrated by Zhu et al. where optimized composites achieved 602 W/(m·K) at 35 vol% loading through tailored carbide interfaces (Zhu et al., 2020). Particle size (>400 μm) synergistically enhances this effect by reducing interfacial scattering sites per unit volume. These findings underscore the necessity of balancing percolation physics with defect minimization for maximizing thermal performance (Feng et al., 2010).

5.3 Sintering parameters

Sintering process parameters significantly influence the thermal conductivity of diamond/copper composites by modulating both intrinsic material properties and interfacial interactions. The sintering temperature directly governs the interdiffusion behavior between diamond and copper matrix, as well as the inherent characteristics of both phases (Kang et al., 2013b). Excessive temperatures (>1,050°C) induce diamond graphitization, whereas optimized interfacial reactions can be achieved through controlled sintering durations (e.g., 9 min), as demonstrated by Xia et al. Furthermore, applied pressure emerges as a critical factor in thermal transport optimization. Enhanced pressure promotes densification through improved diamond-copper consolidation, thereby reducing interfacial defects and elevating thermal conductivity (Lei et al., 2020; Wang et al., 2020). Ciupiński et al. (2017) achieved a maximum thermal conductivity of 687 W m^{-1}·K^{-1} in chromium-coated diamond/copper composites by optimizing pulsed plasma sintering parameters, specifically employing a sintering temperature of 850°C with a 10-min holding time.

6 Discussion

6.1 Interfacial engineering synergy

Surface metallization techniques (e.g., TiC/WC interlayers via magnetron sputtering) establish chemically bonded interfaces that simultaneously enhance wettability and suppress thermal boundary resistance (TBR <10^{-8} m^2 K·W^{-1}). These layers mitigate phonon scattering by reducing interfacial defects, as evidenced by the 846.5 W m^{-1}·K^{-1} achieved in vacuum-metallized composites. Matrix alloying complements this approach: Zr doping (0.5 wt%) generates discontinuous ZrC nanostructures (two to five nm) that enable phonon impedance matching, pushing thermal conductivity to 930 W m^{-1}·K^{-1}. Crucially, the synergy between carbide crystallography (e.g., Cr_7C_3 vs. Cr_3C_2) and sintering dynamics (e.g., pressure-assisted recrystallization) dictates interfacial coherence, with graded architectures (W_2C/WC) demonstrating superior phonon transmission.

6.2 Process-defect interplay

While high-pressure sintering and melt infiltration achieve dense composites (>740 W m^{-1}·K^{-1}), their scalability is hampered by energy-intensive protocols. Spark plasma sintering (SPS) offers rapid densification but introduces interfacial porosity (5–15 vol%), underscoring the trade-off between process efficiency and microstructural perfection. The thermal transport hierarchy—dictated by diamond size (>400 μm), loading (60–70 vol%), and surface roughness—reveals a percolation threshold: exceeding 70 vol% disrupts copper infiltration, while suboptimal sintering temperatures (>1,050°C) trigger graphitization-dominated failure. These phenomena highlight the necessity of multiscale parameter coupling, where atomic-scale interface design must align with macroscopic process constraints.

Despite progress, critical challenges persist: (1) Multi-property synergy—mechanical robustness must be reconciled with ultrahigh conductivity; (2) Cost-effective fabrication—emerging techniques like additive manufacturing require development to circumvent high-energy processes; (3) Atomic-level interface engineering—crystallographic orientation effects of carbide layers on phonon scattering demand fundamental exploration (4) Industrial translation—metallization protocols (e.g., molten salt, vacuum plating); necessitate parameter standardization for large-area production. Current limitations in diamond/Cu composites include inadequate interface phonon control, high-energy fabrication dependence, and non-standardized industrial protocols. Future directions demand: ML-guided carbide gradients with topological diamond architectures, laser-assisted cold spray additive manufacturing, and plasma-enhanced infiltration for defect-free interfaces. Quantum-enabled thermal mapping via NV centers and digital twin-assisted metallization could establish ZT-like standards, bridging atomic engineering to scalable production.

7 Conclusion

This review highlights interfacial engineering and process optimization as critical enablers for diamond/copper composites in high-power electronics. Surface metallization and matrix alloying synergistically enhance bonding and reduce thermal resistance via carbide layers and phonon transport optimization. While HPHT sintering and melt infiltration yield high-density composites, scalability and cost barriers remain. Precise control of diamond morphology, size (>400 μm), volume fraction (60–70 vol%), and sintering parameters is essential to maximize thermal conductivity (>900 W/(m·K)) and minimize defects. Future work must prioritize hybrid strategies (e.g., surface roughening with multilayered coatings), scalable manufacturing, and interfacial phonon dynamics to meet next-generation microelectronics demands. The synergistic integration of interfacial phonon engineering with hierarchical multiscale architectures (nanoscale interface design to macroscale structural optimization) represents the fundamental strategy to overcome thermal transport barriers exceeding 1000 W/(m·K) in next-generation thermal management composites.

Author contributions

YX: Writing–original draft. RL: Writing–original draft. Yongru Deng: Investigation, Supervision, Writing–review and editing. ZZ: Writing–review and editing. JC: Investigation, Writing–review and editing. AM: Writing–review and editing. Ruilong Wen: Writing–review and editing.

Funding

The author(s) declare that financial support was received for the research and/or publication of this article. This work was also supported by the Scientific Research Program of Shaanxi Provincial Science and Technology Department (2024JC-YBQN-0592).

Acknowledgments

The authors thank Xi'an Technological University for the support of this work.

Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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Publisher's note

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frontiers | Frontiers in Materials

TYPE Mini Review
PUBLISHED 30 July 2025
DOI 10.3389/fmats.2025.1655566

OPEN ACCESS

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RECEIVED 28 June 2025
ACCEPTED 16 July 2025
PUBLISHED 30 July 2025

CITATION
Liu Z, Yang X, Jia Y, Zhang Y, Pang Y and Huang X (2025) Research progress in the relationship between packaging structures and service performance of MEMS inertial sensors.
Front. Mater. 12:1655566.
doi: 10.3389/fmats.2025.1655566

Research progress in the relationship between packaging structures and service performance of MEMS inertial sensors

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In recent years, micro-electro-mechanical systems (MEMS) technology has advanced rapidly, leading to widespread adoption of MEMS inertial sensors in areas such as consumer electronics, industrial automation, national defense, and military systems. These sensors offer notable advantages, including compact size, low cost, and ease of large-scale production. This study provides a comprehensive review of recent research, both domestic and international, focusing on how variations in packaging design affect the performance of MEMS inertial sensors across consumer-grade, industrial-grade, and tactical-grade classifications. Typical sensor models, including the MPU9250, ADIS16470, and the tactical-grade HG1930, are selected as representative examples. The influence of different packaging types—such as quad flat no-lead (QFN), ceramic leadless chip carrier (LCC), and hermetic metal vacuum packaging—on key performance metrics such as bias stability, noise density, and temperature drift is analyzed in depth. Moreover, the influence mechanism of electronic packaging design on inertial sensors is explained from the perspective of the coupling of thermal-mechanical-electrical multi-physics models. Finally, this paper explores the development potential of emerging packaging technologies, including heterogeneous integration, intelligent compensation, and quantum-level techniques, in driving future performance breakthroughs in MEMS inertial sensors.

KEYWORDS

packaging structure, MEMS, inertial sensors, service performance, IMU

1 Introduction

As the core components of modern inertial navigation and motion sensing systems, MEMS inertial sensors play a critical role in determining the reliability and performance of applications such as unmanned aerial vehicle (UAV) attitude control, industrial robot positioning, and vehicle navigation systems (Contreras et al., 2025; Li et al., 2024). Currently, market demand for MEMS inertial sensors exhibits a trend of polarization. On one end, consumer-grade products emphasize

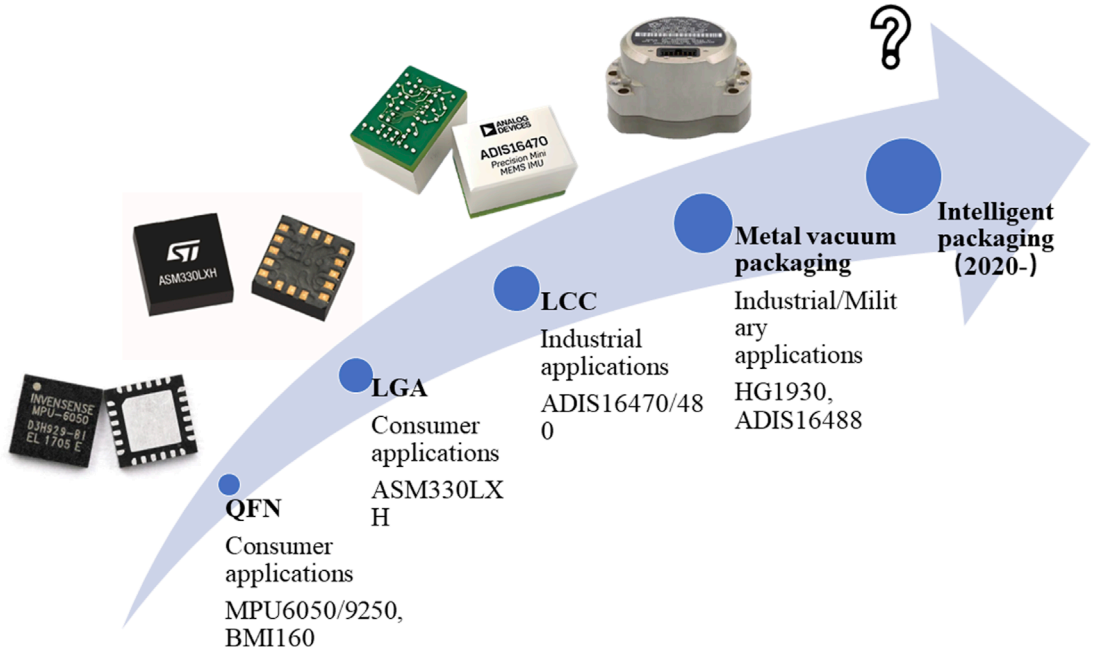

FIGURE 1
The evolution of packaging structures for MEMS inertial sensors.

aggressive cost reduction and further miniaturization. On the other, industrial-grade and tactical-grade devices are pushing performance boundaries toward arcsecond precision levels (Senhaji-Mouhaddib et al., 2024; Harindranath and Arora, 2024). Especially, tactical-grade inertial sensors have higher accuracy and more complex working conditions, often involving small military drones and armored vehicles. Packaging design has emerged as a key factor affecting critical parameters such as bias stability, noise density, and long-term reliability (Del Sarto, 2022; Yang et al., 2024). The evolution process of packaging structures for MEMS inertial sensors can be seen in Figure 1.

The packaging of MEMS inertial sensors has undergone three distinct developmental stages. In the early phase (2000–2010), epoxy molding compound (EMC) packaging was predominant, facilitating the widespread adoption of MEMS sensors in consumer electronics due to its low-cost and scalable manufacturing processes (Yang et al., 2024; Schreier-Alt et al., 2011). During the intermediate phase (2010–2020), the commercialization of ceramic packaging and three-dimensional stacking technologies significantly enhanced the performance of industrial-grade sensors, achieving improvements in accuracy by one to two orders of magnitude (Dean et al., 2011; Dong et al., 2015). In the current stage (2020 to present), advances in vacuum sealing, heterogeneous integration, and intelligent packaging have enabled tactical-grade devices to approach the quantum noise limit (Gong et al., 2024; Edinger et al., 2023; Lau, 2023). This substantial performance improvement has been accompanied by a transition in packaging materials from epoxy resin to titanium alloy, and a shift in the internal environment from atmospheric pressure to ultra-high vacuum conditions (InvenSense, 2016; Analog Devices, 2019; Honeywell, 2018).

However, the underlying correlation mechanisms between packaging design and precision performance have yet to be systematically deconstructed. Most existing studies tend to focus on the localized optimization of individual packaging parameters, such as thermal resistance or the coefficient of thermal expansion (CTE) (Qi et al., 2025), while lacking a comprehensive analysis of the coupled effects arising from thermal, mechanical, and electrical multiphysics interactions. For instance, although CTE mismatch in polymer-based packaging materials is widely acknowledged as a primary contributor to temperature-induced drift in consumer-grade sensors, recent experimental findings indicate that moisture ingress at the packaging interface can induce plastic deformation in these materials (Han et al., 2023), thereby exacerbating the nonlinear drift in long-term bias. Similarly, while the ceramic substrates commonly used in industrial-grade sensors help mitigate thermal stress, their inherently high stiffness can amplify the transmission of external mechanical vibrations, leading to modal coupling and interference with the MEMS structure (Nia and Kouki, 2024). In the case of tactical-grade sensors, although vacuum packaging effectively suppresses gas damping noise, the ultra-high vacuum environment can trigger material outgassing, contaminating the MEMS surface and resulting in a gradual, time-dependent degradation of the quality factor (Guo et al., 2021).

This study selects three representative MEMS inertial sensors at different performance levels—consumer-grade (MPU9250), industrial-grade (ADIS16470), and tactical-grade (HG1930)—to systematically review and analyze the relationship between packaging structure and service performance. The discussion is carried out from multiple perspectives, including material properties, structural topology, and process parameters, in order to clarify how packaging influences key performance characteristics across different precision tiers. The findings aim to provide a technical foundation and design reference for future MEMS packaging solutions in high-performance application scenarios.

TABLE 1 Comparison of packaging structures for three typical MEMS inertial sensors.

Types	QFN	LCC	Metal vacuum packaging
Material	Plastic (Epoxy resin)	Ceramics	Metal (Kovar alloy/Titanium alloy)
Airtightness	None	High	Extremely high
Mechanical strength	Low	High	Extremely high
Thermal performance	Medium	Excellent	Excellent
Bias instability (Allan variance)	≈50°–100°/h	≈10°/h	< 1°/h
Cost	Low	Medium	Extremely high
Typical products	MPU6050/9250, BMI160	ADIS16480/16470, MS9000	HG1930, STIM300

2 Packaging technology for MEMS inertial sensors

The packaging of MEMS inertial sensors plays a pivotal role in maintaining their performance stability and operational reliability. Beyond its basic function as a physical enclosure, packaging can mitigates environmental disturbances and filters internal noise sources (Xu et al., 2024).

In the consumer electronics sector, QFN and Land Grid Array (LGA) packages are the dominant formats for MEMS inertial sensors. For instance, the MPU9250 developed by InvenSense utilizes a compact $4 \times 4 \times 1\,mm^3$ QFN package, which is widely integrated into smartphones, wearable devices, and other portable electronics due to its small footprint and lightweight design (Mischie and Matiu-Iovan, 2024). However, the epoxy molding compound used in this type of packaging exhibits a high coefficient of thermal expansion, which significantly mismatches that of the silicon-based MEMS chip. During thermal cycling, this mismatch generates considerable interfacial shear stress, leading to mechanical deformation and stiffness drift in the MEMS cantilever structures. Such effects substantially degrade sensor accuracy and limit the applicability of QFN-packaged sensors in thermally sensitive environments (Hollstein et al., 2021).

Compared to consumer-grade products, industrial-grade MEMS inertial sensors impose stricter requirements on packaging reliability and long-term stability. A representative example is the ADIS16470 developed by Analog Devices, which employs a Ceramic Leadless Chip Carrier (CLCC) package (Analog Devices, 2019). The alumina ceramic substrate used in this design has a CTE of approximately 6.5 ppm/°C, closely matching the thermal expansion behavior of silicon-based MEMS structures. In addition, low-stress bonding using gold-tin (Au80Sn20) eutectic solder significantly reduces thermally induced deformation by over 60%, thereby enhancing both sensor performance and durability under complex industrial operating conditions. The hermetic nature of CLCC packaging further contributes to environmental robustness, offering effective protection against dust, moisture, and corrosive gases commonly encountered in industrial settings (Chen Y. et al., 2022).

In tactical applications where exceptional accuracy and stability are required, MEMS inertial sensors are typically enclosed in metal housings made of titanium alloys or Kovar (Honeywell, 2018). These packaging materials provide outstanding mechanical strength and electromagnetic shielding, while enabling high-vacuum environments to effectively suppress gas damping effects on the MEMS resonant structures. This contributes to enhanced sensitivity and improved resistance to external disturbances, thereby satisfying the stringent performance demands of aerospace and military navigation systems. Furthermore, the thermal conductivity of metal packaging is approximately 40% higher than that of ceramic counterparts, allowing for more efficient heat dissipation during sensor operation and reducing the risk of performance degradation due to localized overheating (Han et al., 2023). To further ensure operational integrity under extreme conditions, tactical-grade packaging commonly incorporates multi-layer stress-buffering structures and redundant design elements (Zotov et al., 2021; Analog Devices, 2014), which help maintain signal integrity and measurement accuracy even under severe mechanical shocks (e.g., accelerations exceeding 10,000 g) and wide operating temperature ranges from −55°C to 125°C. The performance and features comparison of packaging structures for three typical MEMS inertial sensors can be seen in Table 1.

3 The influence mechanism of packaging technology

3.1 Thermal management capability

The thermal conductivity of packaging structures plays a critical role in maintaining temperature uniformity within MEMS inertial sensors (Hu et al., 2021). For example, the QFN package used in the MPU9250 incorporates plastic encapsulation materials with inherently low thermal conductivity. This results in pronounced axial temperature gradients under continuous power dissipation, which can introduce common-mode errors in the differential capacitance sensing circuitry. In contrast, the ADIS16470 adopts an aluminum nitride ceramic substrate (Analog Devices, 2019), known for its high thermal conductivity, in combination with integrated heat pipe technology. This design effectively mitigates internal temperature differentials and significantly reduces thermal gradient-induced measurement errors.

Moreover, the thermal hysteresis characteristics of packaging materials can induce nonlinear bias drift in MEMS inertial sensors (Pieniazek and Ciecinski, 2020). In the case of the MPU9250, the plastic encapsulant exhibits significant hysteretic behavior during temperature cycling, leading to residual stress accumulation and measurable deviations in acceleration bias. In contrast, ceramic packaging materials, which possess a high elastic modulus and exhibit a narrow thermal hysteresis loop, produce substantially smaller bias offsets under similar conditions. This inherent material stability contributes to improved thermal repeatability and overall measurement consistency.

3.2 Suppression strategies for mechanical stress

Packaging-induced stress affects MEMS inertial sensor performance through two primary mechanisms (Seok, 2022). First, static stress can modify the stiffness of MEMS structures, leading to variations in sensor output (Das and Bhushan, 2023). For instance, the MPU9250 demonstrates notable sensitivity to packaging-induced stress. Changes in the torque applied to mounting bolts alter the interfacial stress distribution, resulting in significant shifts in bias error. Second, dynamic stress can excite structural resonances within the sensor. Vibrations transmitted through the packaging shell at specific frequencies may couple into the substrate and reach the MEMS proof mass, generating spurious angular rate signals and degrading measurement accuracy.

To mitigate the adverse effects of packaging-induced stress, various technical solutions have been implemented across different sensor grades. The ADIS16470 incorporates a corrugated stress-buffer layer at the base of its package. This design absorbs mechanical stress through localized plastic deformation and simultaneously elevates the packaging's resonance frequency beyond the operational bandwidth of the sensor, thereby minimizing resonance-induced errors. In tactical-grade MEMS sensors, active damping technologies are employed. By embedding piezoelectric ceramic actuators within the package, these systems utilize closed-loop control to actively suppress external vibration inputs in real time, significantly enhancing dynamic stability and measurement fidelity.

3.3 Package optimization for signal integrity

High-frequency noise and EMI are critical factors that constrain the resolution and signal integrity of MEMS inertial sensors (Tehrani and Mojtaba Atarodi, 2024). Conventional wire bonding techniques introduce parasitic inductance, which, in conjunction with the intrinsic capacitance of MEMS structures, can form unintended LC resonance circuits. These resonances amplify the noise power spectral density within specific frequency bands, thereby degrading sensor performance. In contrast, TSV technology offers a substantial improvement by minimizing parasitic inductance. Utilizing silicon dielectric isolation and deep reactive ion etching (DRIE), TSV enables compact vertical interconnections with reduced electrical path lengths, effectively suppressing high-frequency noise and enhancing overall EMI immunity.

In terms of electromagnetic shielding, the effectiveness of a shielding structure is directly related to its ability to attenuate external electromagnetic field interference (Ghanam et al., 2023). For example, the ADIS16470 utilizes a gold–nickel dual-layer shielding configuration. This design strategically exploits the skin effect of gold, which enhances attenuation of high-frequency electric fields, in combination with the high magnetic permeability of nickel, which effectively suppresses low-frequency magnetic components. Compared to conventional single-layer aluminum shielding, this composite structure significantly improves shielding effectiveness across a broader frequency spectrum, thereby enhancing the sensor's resilience to EMI in complex electromagnetic environments.

4 Future trends and challenges

4.1 Wafer level packaging

Wafer Level Packaging (WLP) can integrate MEMS structures and ASICs during the front-end manufacturing process, thereby effectively shortening the interconnection length and reducing parasitic capacitance, typically achieving a reduction of more than 50% (Ghanam et al., 2023; Chen et al., 2022b; Ubando and Gonzaga, 2025), such as STMicroelectronics' ISM330DHCX (ISM330DHCX Datasheet, 2025). Heterogeneous integration methods package optical, radio frequency, and MEMS devices into a unified platform, such as the CHIPS (Common Heterogeneous Integration and IP Reuse Strategy) project initiated by the U.S. Defense Advanced Research Projects Agency (DARPA). It realizes the hybrid integration of photonic integrated circuits and MEMS gyroscopes through an interposer, which greatly improves the angular resolution and signal processing capability for high-performance inertial sensing applications (Zhang et al., 2022).

4.2 Intelligent packaging

Intelligent packaging integrated with artificial intelligence processors is also one of the key directions for the future development of MEMS inertial sensor systems. For example, Bosch's SMI230 series directly integrates a machine learning accelerator within the sensor package (BOSCH, 2024). By modeling and compensating for these influences online, the system effectively mitigates the impact of bias errors on the overall performance of the sensor. Moreover, deep learning-based lifetime prediction algorithms can detect early indicators of degradation phenomena, such as creep at the bonding interface or material aging, thereby providing predictive maintenance capabilities and early fault warning.

4.3 Quantum packaging

To break through the limitations of traditional inertial sensing, quantum inertial sensors require ultra-low temperature and ultra-high vacuum environments at the packaging level. The atomic

interferometer gyroscope developed by the U.S. National Institute of Standards and Technology (NIST) adopts a rubidium atomic gas cell combined with laser cooling packaging to suppress system phase noise under near-vacuum conditions (Milton et al., 2021). However, the perfect realization of such packaging requires solving a series of complex engineering problems, including adiabatic thermal management, multi-layer μ-metal magnetic shielding, and active vibration isolation using optical platforms.

5 Conclusion

This paper systematically reviews the impacts of packaging structures, material selection, and process parameters on the operational performance of MEMS inertial sensors across different precision levels. Through multi-angle and multi-level analysis, it emphasizes the critical role of packaging in mitigating environmental interference, reducing internal noise, and enhancing mechanical stability, while revealing the coupling relationship between electronic packaging technology and the service performance of MEMS inertial sensors.

Meanwhile, this paper also looks ahead to the electronic packaging and signal processing technologies of next-generation inertial sensors, such as wafer-level packaging technology, heterogeneous integration technology, and intelligent packaging technology. Intelligent packaging technology, which realizes real-time compensation and early warning by adopting AI, will further promote the development of sensors towards adaptive intelligence in the future. These innovative technologies will be crucial for meeting the stringent requirements of advanced application fields such as autonomous navigation, deep space exploration, and quantum positioning systems.

Author contributions

ZL: Funding acquisition, Methodology, Writing – original draft, Writing – review and editing. XY: Conceptualization, Funding acquisition, Methodology, Project administration, Supervision, Writing – original draft, Writing – review and editing. YJ: Investigation, Resources, Writing – original draft. YZ: Investigation, Resources, Validation, Writing – original draft. YP: Software, Validation, Visualization, Writing – original draft. XH: Formal Analysis, Investigation, Validation, Writing – original draft.

Funding

The author(s) declare that financial support was received for the research and/or publication of this article. This research is supported by the Shaanxi Provincial Natural Science Basic Research Program (2025JC-YBMS-542), Scientific Research Program of Shaanxi Provincial Department of Education (24JR048, 24JK0383), Xianyang Innovation Capability Support Program - Excellent Innovation Team Program (L2024-CXNL-KJRCTD-KJTD-0009) and Scientific Research Projects of Shaanxi Energy Institute (2024KYTD05, 2024KYZRP04QN).

Conflict of interest

Author XH was employed by Beijing Aerospace Times Optical-Electronic Technology Co., Ltd.

The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Generative AI statement

The author(s) declare that no Generative AI was used in the creation of this manuscript.

Publisher's note

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frontiers | Frontiers in Materials

TYPE Original Research
PUBLISHED 14 August 2025
DOI 10.3389/fmats.2025.1668151

OPEN ACCESS

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RECEIVED 17 July 2025
ACCEPTED 29 July 2025
PUBLISHED 14 August 2025

CITATION
Jia Y, Xue H and Wang Z (2025) Research on hydrogen induced cracking behavior and service performance of metal pipeline material.
Front. Mater. 12:1668151.
doi: 10.3389/fmats.2025.1668151

Research on hydrogen induced cracking behavior and service performance of metal pipeline material

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This study systematically investigates the fracture behavior of X80 pipeline steel welded joints under hydrogen-induced cracking (HIC) conditions through combined experimental characterization and numerical simulation. Microstructural observations and Vickers hardness testing reveal significant heterogeneity in the base metal, heat-affected zone (HAZ), and weld metal (WM), resulting in spatially non-uniform mechanical properties. A user-defined subroutine (USDFLD) was employed to assign continuous material property distributions within the finite element model, accurately capturing mechanical heterogeneity and its influence on crack-tip mechanical fields and crack propagation paths. Results show that welding thermal cycles induce pronounced microstructural evolution, significantly altering hardness and strength distributions, which in turn affect the evolution of crack-tip stress and plastic strain fields. Crack propagation preferentially occurs toward regions of higher yield strength, where limited plasticity leads to intensified crack-tip stress concentration, accelerating crack growth and extending propagation paths. Moreover, crack growth is accompanied by local unloading near the crack tip, reducing peak stress and strain compared to the initial stationary crack tip. The stress and strain field reconfiguration are primarily localized near the crack tip, while the far-field mechanical response remains largely stable.

KEYWORDS

pipeline steel, welded joint, microstructure, hic, crack propagation

1 Introduction

With the strategic role of hydrogen energy rising in the global energy transition, hydrogen transmission pipelines—serving as essential infrastructure for large-scale and efficient hydrogen transport—are entering a phase of accelerated engineering deployment. Compared with compressed hydrogen tanks and liquid hydrogen transportation, pipeline transmission offers distinct advantages such as high continuity, low transport cost, and superior energy efficiency, making it one of the primary methods for medium- and long-distance hydrogen delivery (Li et al., 2021; Benjamin et al., 2016). Hydrogen's high diffusivity and embrittling nature pose severe reliability challenges to transmission pipelines under complex service conditions. High-strength pipeline steels are prone to degradation in mechanical properties during long-term service, and hydrogen ingress may induce HIC, potentially leading to sudden failure events (Sun and Cheng, 2018;

Wang et al., 2024a). Statistics show that the coexistence of microstructural defects, hydrogen-rich environments, and external loading can easily trigger typical environmentally assisted cracking (EAC) phenomena such as HIC, posing a significant threat to the structural integrity and operational safety of hydrogen pipelines (Wang et al., 2025a). A comprehensive understanding of the mechanical response and crack propagation behavior of high-grade pipeline steels under high-pressure hydrogen is essential to ensure the reliability of hydrogen transmission pipelines.

Currently, most hydrogen transmission pipelines rely on welded joints for long-distance continuous deployment. Due to the influence of welding thermal cycles and metallurgical transformations, the WM and its adjacent heat-affected zone (HAZ) exhibit significant differences in microstructure and mechanical properties compared to the base metal (Xie et al., 2020), which increases the uncertainty in crack propagation paths and complicates defect assessment and life prediction for welded joints. In engineering practice, the minimum yield strength is typically specified based on the grade of the base metal. However, actual yield strength often exhibits considerable variation, making traditional assumptions of "even-matched" or "over-matched" welds increasingly inadequate for accurate assessment (Zhu et al., 2017; Ayrault et al., 2011). Yang et al. (2015) investigated the fracture resistance of X80 pipeline welds using CTOD and J-integral tests, identifying the fusion zone as a crack-prone region, where the presence of M–A constituents was a critical factor in reduced toughness. Kim et al. (2005) reported that X80 steel, owing to its refined acicular ferrite and polygonal ferrite microstructure, demonstrated excellent low-temperature toughness and weldability; its HAZ also exhibited good impact resistance under high-pressure conditions. Xu et al. (2020) employed finite element analysis to study the effect of weld cap removal on fatigue performance, revealing that reducing stress concentration at the weld toe could effectively delay crack initiation and extend fatigue life, highlighting the critical role of weld geometry. However, most existing studies treat welded joints using simplified, homogeneous partitioned models, neglecting the non-uniform and abrupt transition characteristics across the weld interfaces. Xue et al. (2021) attempted to introduce a continuously graded material model using UMAT, which improved simulation accuracy to some extent, but the approach involved complex implementation and frequent convergence issues. To address these limitations, this study develops a user-defined USDFLD subroutine within ABAQUS to build an efficient, engineering-focused model with continuously varying material properties across welded joints. This model enables high-fidelity simulation of crack-tip mechanical behavior in high-strength pipeline steels under high-pressure hydrogen, providing a solid basis for assessing hydrogen-induced cracking risk.

Due to the highly localized and variable mechanical states at crack fronts in welded structures, accurately capturing the stress–strain evolution in the crack-tip microregion under high-pressure hydrogen environments is essential for predicting HIC propagation paths and evaluating structural integrity (Xue et al., 2021; Wang et al., 2023; Xue et al., 2011). To address this challenge, various experimental and numerical approaches have been developed to investigate weld integrity in hydrogen-embrittlement-prone environments (Shoji et al., 2010; Peng et al., 2011; Dong et al., 2018). Burstow et al. (1998) utilized a modified boundary layer (MBL) method in a 2D plane strain finite element model to simulate cracks within WM aligned parallel to the interface. By adjusting the T-stress and base metal strength, they examined geometric constraints and material mismatch effects, proposing a normalized loading parameter to quantify constraint across different mismatch conditions. Their results indicated that overmatched welds exhibit constraint behavior similar to homogeneous materials, whereas undermatched welds show high sensitivity to loading parameters, sometimes even surpassing homogeneous constraints. (Betegón and Peñuelas (2006) introduced a constraint parameter β_m to quantify mismatch effects in overmatched welds, and further proposed a combined constraint parameter β_T incorporating both geometric and material factors to support safety margin evaluations for high-strength welds in hydrogen environments. Štefane et al. (2019) integrated experimental testing with finite element simulations to reveal the evolution of crack-tip triaxiality in bi-material welded joints under hydrogen permeation. Their study highlighted that neglecting material mismatch and hydrogen–metal interactions in fracture assessments may lead to inaccurate evaluations of weld toughness. Similarly, Wang et al. (2024b) performed comprehensive numerical simulations in ABAQUS to investigate the crack-tip field evolution from initiation to propagation at different locations within dissimilar metal welds, providing new insights into HIC propagation rate prediction. In summary, the refined modeling and parameterization of material heterogeneity, geometric constraints, and hydrogen–metal coupling effects—considering the specific challenges of high-pressure hydrogen service—represent a forward-looking research direction for improving the accuracy of safety design and life assessment in hydrogen pipeline systems.

This study systematically investigates welded joints of X80 high-strength pipeline steel. Metallographic analyses clarify phase transformation mechanisms driving microstructural heterogeneity and HIC susceptibility. Micro-indentation hardness mapping quantifies spatial mechanical variations, underpinning a USDFLD subroutine that continuously assigns mechanical properties in finite element simulations. Combined with crack growth criteria, numerical results reveal how property gradients steer crack propagation and influence crack-tip fields. These findings establish a robust theoretical and modeling framework for integrity assessment and service life prediction of high-grade hydrogen pipelines under high-pressure operation.

2 Materials and methods

2.1 Materials and specimens

High-pressure hydrogen transmission places stringent demands on the structural integrity of welded joints, particularly in high-strength steels where significant mechanical property mismatches often exist between the WM and base metal. Such heterogeneity can serve as a critical zone for the initiation and propagation of HIC. The welded joint investigated in this study was obtained from an in-service X80-grade hydrogen transmission pipeline. Its configuration consists of a typical butt joint between X80 base metals joined by a circumferential weld. The geometric structure and dimensions of the specimen are shown in Figure 1. As illustrated in Figure 1a, the outer diameter of the pipe section is 1,219.0 mm with a wall thickness

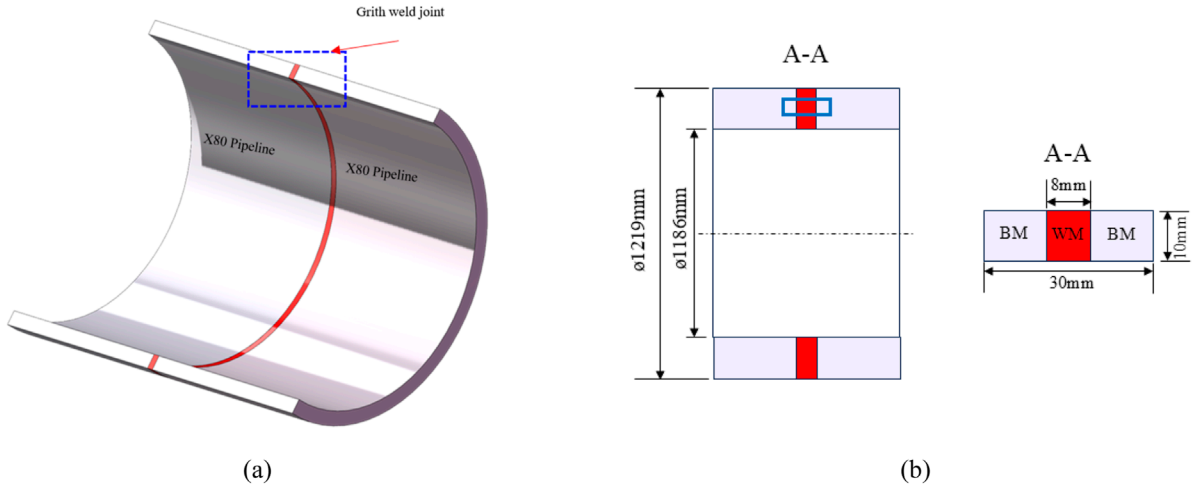

FIGURE 1
Structure of the X80 pipeline steel welded joint. **(a)** X80 pipeline steel welded joint **(b)** Material regions of the welded joint.

TABLE 1 Compositions of X80 steel base metal and weld (mass fraction/%).

Materials	C	Si	Mn	Ni	Cr	Cu	Nb	Al	Mo	S	P	Fe
Base metal	0.055	0.071	1.80	0.136	0.007	0.262	0.042	0.005	0.264	0.001	0.016	Bal
Weld	0.022	0.126	1.03	0.787	0.018	0.045	0.010	0.995	0.034	0.002	0.018	Bal

of 16.5 mm, which conforms to standard design specifications for modern large-diameter hydrogen transmission pipelines.

The chemical composition of the WM, expressed in weight percent, is listed in Table 1, serving to reveal the potential influence of alloying elements on mechanical performance and hydrogen sensitivity. All specimens were extracted along the axial direction of the pipe and sectioned perpendicular to the circumferential weld to ensure the weld region was centered within each sample. This configuration facilitates a systematic analysis of the microstructural and mechanical differences among the base metal (BM), HAZ, and WM under hydrogen exposure, thereby providing a reliable basis for subsequent mechanical characterization and hydrogen embrittlement assessment.

2.2 Metallographic analysis

Welded joint specimens were extracted from the weld region of the pipeline steel. Surface preparation was carried out using an automated grinding and polishing machine, with final polishing down to 0.2 μm to minimize measurement error. The grinding/polishing wheel was operated at a rotational speed of 1,000 r/min. To remove surface oxides, 200-grit abrasive paper was used initially, followed by sequential fine grinding with 400-, 800-, and 1200-grit papers. Mirror polishing was completed using a polishing cloth and diamond suspension to ensure high surface quality and testing consistency. The specimen preparation process is illustrated in Figure 2.

After polishing, the weld cross-section was etched using a 4 wt% nitric acid–ethanol solution. Following etching, the samples were rinsed, dried, and subjected to microstructural examination using an optical microscope (OM). Representative micrographs were obtained from positions "A" to "C" as indicated in Figure 2.

2.3 Local mechanical tests

To evaluate the local mechanical properties across different regions of the X80 welded joint, miniature flat tensile specimens were fabricated from the joint cross-section using electrical discharge machining (EDM), as shown in Figure 3. Each specimen had a thickness of 2 mm, a width of 3 mm, and a gauge length of 20 mm.

Specimens were extracted from the base metal (No. 1), HAZ (No. 2), and WM (No. 3), with the loading direction parallel to the weld interface to simulate the actual service stress orientation. The specimen layout and numbering are shown in Figure 4. This configuration was designed based on microstructural continuity and stress gradient considerations to reveal the transition in mechanical properties and provide input parameters for subsequent finite element modeling and hydrogen-induced cracking analysis.

During uniaxial tensile testing, specimen deformation was monitored in real time using a high-precision static strain measurement system with a range of ±65,000 με, resolution of 0.2 με, and measurement error within ±2 με or 0.4% of the reading, ensuring accurate data acquisition at small strain levels. All miniature tensile tests were conducted on a hydraulic servo loading system with a ±60 kN rated load, maximum operating pressure of 22 MPa, and flow rate of 28 L/min, providing stable loading and fine control suitable for small metallic specimens.

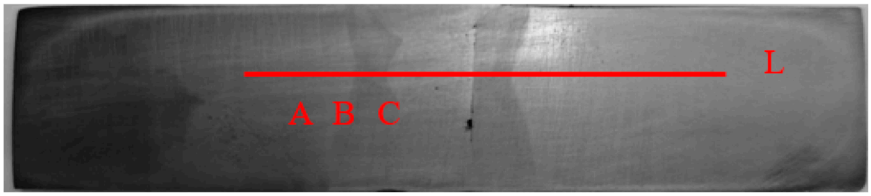

FIGURE 2
Locations for microstructural observation (A to C) and microhardness measurement (along line L).

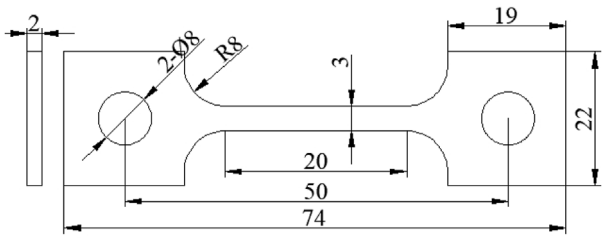

FIGURE 3
Dimensions of flat tensile specimens for local mechanical testing.

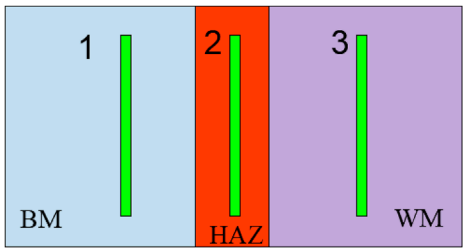

FIGURE 4
Positions of the three flat tensile specimens in the X80 welded joint.

Engineering stress–strain curves from each region were obtained to characterize the local mechanical behavior of the welded joint. For subsequent finite element modeling, experimental data were converted to true stress and true strain using Equations 1 and 2 to better capture material response at large strains.

$$\varepsilon = \ln\left(1+\varepsilon_e\right) \tag{1}$$

$$\sigma = \sigma_e\left(1+\varepsilon_e\right) \tag{2}$$

2.4 Microhardness testing

To characterize hardness distribution across different regions of the welded joint, systematic hardness measurements were conducted following the GB/T 2654—2008 "Welded Joint Hardness Testing Method" and GB/T 4340—2009 "Metal Vickers Hardness Test" standards. A micro-Vickers hardness tester equipped with an automatic turret and image recognition system was used to enable intelligent control and high-precision readings throughout the testing process. Prior to testing, specimen surfaces were mechanically ground and mirror-polished to remove oxides and surface defects. Hardness measurements covered the base metal, HAZ, and WM regions. All tests utilized an automatic loading/unloading program with a load of 196 gf (approximately 200 g) and a dwell time of 15 s. The image system identified the indentation morphology and calculated diagonal lengths to determine hardness values.

Indentation points were arranged along the cross-section with a spacing of 0.5 mm, allowing high-resolution mapping of hardness gradients across different zones.

3 Finite element simulation

3.1 USDFLD subroutine and crack propagation theory

3.1.1 USDFLD subroutine

In this study, material properties (such as stress, strain, and strain rate) are defined as functions of field variables $f(i)$. The mechanical behavior at the integration points of finite elements is linked to the field variable functions $f(i)$, enabling a more realistic representation of the spatial variation of material properties within the dissimilar metal welded joint (DMWJ).

Initially, material mechanical characteristics are associated with the field variables. During the subroutine initialization, the program obtains the coordinates COORD(i) of the welded joint, mapping these spatial coordinates to the corresponding field variables $f(i)$, which in turn are linked to state variables STATEV(i) (Wang et al., 2024b; Xue et al., 2024). This approach ultimately enables the characterization of heterogeneous mechanical properties within the joint (Zhao et al., 2025).

3.1.2 Crack propagation based on crack-tip opening stress

To simulate the non-steady-state propagation of HIC under the coupled effects of high-pressure hydrogen environment and mechanical loading, this study develops a crack growth criterion based on Crack-Tip Opening Stress (CTOS), implemented in the ABAQUS finite element platform via the user subroutines USDFLD. The method assumes that hydrogen accumulates at the crack tip,

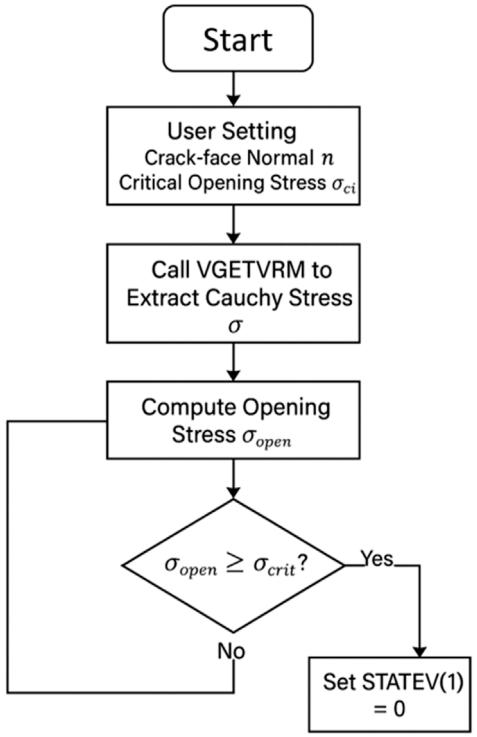

FIGURE 5
USDFLD flow.

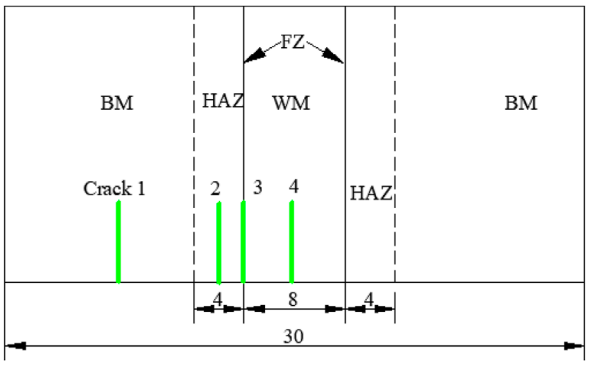

FIGURE 6
Schematic diagram of different regions in the X80 pipeline steel welded joint.

weakening metallic bonds, making the normal principal stress the dominant driving force for crack growth. In this study, the critical opening stress (σ_{crit}) is set as 528 MPa, corresponding to the measured yield strength of the WM. This value was used as a uniform failure criterion across the welded joint to ensure a conservative assessment of crack initiation. When the opening stress σ_{open} as shown in Equation 3 in the normal direction exceeds the material's critical threshold σ_{crit} under hydrogen exposure, localized damage occurs, promoting crack propagation.

Within each loading increment, the Cauchy stress tensor σ at the integration point is extracted using GETVRM and projected onto the unit normal vector n of the crack plane to calculate the opening stress as:

$$\sigma_{open} = n^T \cdot \sigma \cdot n = \sum_{i=1}^{3}\sum_{j=1}^{3} n_i \cdot \sigma_{ij} \cdot n_j \quad (3)$$

This expression represents the tensile normal stress perpendicular to the crack plane, reflecting the local opening stress at the crack tip. The computed σ_{open} is compared against the critical opening stress σ_{crit}. If $\sigma_{open} > \sigma_{crit}$, the corresponding integration point's state variable STATEV (1) (or field variable FIELD (1)) is set to zero, indicating that the damage criterion is met. This triggers crack extension mechanisms such as element failure, crack surface activation, or cohesive interface release. The computational flowchart is shown in Figure 5.

This model preserves the mechanically dominated characteristics based on opening stress and is well suited for simulating dynamic hydrogen-induced crack propagation in heterogeneous structures such as dissimilar metal welded joints. Combined with the crack-tip submodel technique, it accurately captures crack-tip stress evolution and microscale damage behavior while maintaining computational efficiency.

3.2 Geometry and crack locations

The simplified schematic of the X80 pipeline steel welded joint used in the finite element simulations is shown in Figure 6. In actual engineering practice, the weld interface typically exhibits geometric curvature and a metallurgical diffusion zone rather than an ideal flat boundary. To reduce modeling complexity, the weld region is simplified with a perfectly planar interface in this study. To analyze the influence of mechanical gradients at the heterogeneous joint on the evolution of crack-tip stress–strain fields and to investigate local failure mechanisms at the interface, multiple initial cracks were introduced at the interface and its adjacent regions.

Near the weld interface, initial crack locations were sequentially arranged within the X80 BM, HAZ, BM/HAZ boundary, and the WM center. As illustrated in Figure 6, the y-axis is defined as the spatial coordinate normal to the interface, with y representing the crack positioned at the interface center.

Based on the USDFLD subroutine that implements a continuous spatial distribution of material properties, four representative initial crack paths were selected to reflect the impact of interface heterogeneity on crack propagation behavior. The crack locations are detailed in Figure 6 and summarized in Table 2.

3.3 Mesh and boundary conditions

To investigate the influence of mechanical heterogeneity on crack-tip fields, a two-dimensional finite element model was established, consisting of: (i) crack-tip stress–strain field analysis, and (ii) crack propagation path simulation.

For the crack-tip field analysis, an initial crack length of $a = 3.0\,mm$ was set. The crack tip was modeled using collapsed quadrilateral elements with a midpoint node parameter of 0.25. The mesh near the crack tip region ($r = 0.2\,mm$) was refined to

TABLE 2 Locations of four initial cracks in the weld interface region of X80 pipeline steel.

Crack no.	Location
1	BM
2	HAZ
3	Interface
4	WM

an element size of 0.0025 mm, employing four-node plane strain elements (CPE4), as shown in Figure 7a.

Crack propagation was simulated using a custom user field subroutine (USDFLD), which dynamically updates local material mechanical properties in the finite element model, enabling continuous evolution of properties near the crack tip and simulation of crack path growth. A constant stress intensity factor $\left(30\mathrm{MPa\,m}^{1/2}\right)$ was applied to mimic stable crack growth under service conditions.

4 Results and discussion

4.1 Microstructure of the X80 pipeline steel welded joint

Figure 8a shows that the X80 base metal primarily consists of regularly arranged polygonal ferrite and fine granular bainite. The ordered distribution of ferrite imparts good toughness and ductility to the material, while the fine particulate bainite exhibits strong corrosion resistance.

Figure 8b illustrates the microstructural changes in the HAZ and at the weld interface. Due to the high heat input during welding and the fusion of different materials, significant microstructural transformations occur in this region, including the partial conversion of ferrite into columnar grains. The elongated morphology and larger size of these columnar grains create a weak zone at the weld edge, which is prone to crack initiation and often serves as the actual fracture origin.

Figure 8c depicts the microstructure at the weld center. Temperature gradients and cooling rate variations during welding lead to partial grain coarsening, while rapid cooling inhibits recrystallization and grain refinement, resulting in heterogeneous grain size distribution. These microstructural differences across regions significantly influence the local mechanical properties of the welded joint.

4.2 Local mechanical properties of the X80 welded joint

Miniature flat tensile specimens were extracted from the BM, HAZ, and WM of the X80 welded joint to measure local mechanical properties. Figure 9a shows the engineering stress–strain curves for BM, HAZ, and WM. Using Equations 1 and 2, the true stress–strain curves for the local regions of the X80 welded joint were obtained, as presented in Figure 9b. The stress-strain curve fitting equations for WM, HAZ, and BM are shown in Equation 4

$$\sigma_y = \begin{cases} 528 + 1504.9 * \varepsilon(\mathrm{WM}) \\ 566 + 1206.7 * \varepsilon(\mathrm{HAZ}) \\ 598 + 1199.7 * \varepsilon(\mathrm{BM}) \end{cases} \tag{4}$$

The mechanical properties of the X80 pipeline steel welded joint were preliminarily evaluated by Vickers hardness testing, with the hardness distribution shown in Figure 10. The results indicate that thermal cycling during welding reduces dislocation density and causes precipitate coarsening, leading to softening in the critical and fine-grained zones, exhibiting a typical "V"-shaped hardness profile. The BM, relatively unaffected by heat input, maintains a high hardness level of approximately 296 ± 2 HV. In contrast, the HAZ shows significant hardness reduction, averaging 209 ± 5 HV, reflecting grain coarsening and thermal softening. The WM hardness gradually increases from 208 HV to about 287 HV, indicating its distinct microstructural state. The high hardness of the X80 BM and the softening in the HAZ highlight the critical roles of material composition, heat input, and strength matching in influencing softening degree. A pronounced hardness gradient exists between the WM and HAZ, and such mechanical heterogeneity can more readily induce HIC under high-pressure hydrogen environments, making the interface region a sensitive site for crack initiation and propagation.

The international standard ISO 15653:2018 provides a technical basis for evaluating the mechanical properties of different regions within welded joints (ISO 15653:2018, 2018). The conversion relationships between hardness and mechanical properties established by this standard enable a relatively accurate estimation of the mechanical property distribution in both the BM and the WM (Wang et al., 2025b). This approach has been widely applied to various engineering materials, including alloy steels, nickel-based alloys, and stainless steels. The correlations between hardness and strength are presented in Equations 5 and 6. The distributions of yield strength and tensile strength along the X80 pipeline steel welded joint are shown in Figures 11a,b.

$$\sigma_y = 2.35HV + 62 \tag{5}$$

$$\sigma_u = 3.0HV + 22.1 \tag{6}$$

Based on these hardness-strength conversion relations, the strength distribution at various locations in the X80 welded joint was calculated. By substituting the local yield strength into Equation 1, the corresponding stress–strain curve at each point was obtained. Subsequently, these location-dependent stress–strain data were assigned to the finite element model via the USDFLD subroutine, enabling a continuous spatial mapping of mechanical properties throughout the welded joint.

4.3 Crack-tip mechanical fields at different locations of the welded joint

Figure 12 presents the distribution of von Mises stress at the crack tips located in different regions of the welded joint.

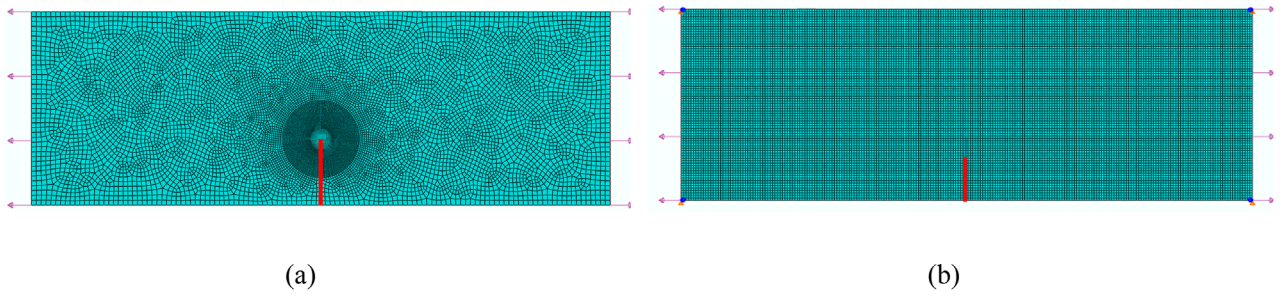

FIGURE 7
Mesh model: **(a)** Crack-tip stress–strain field analysis; **(b)** Crack propagation mesh model.

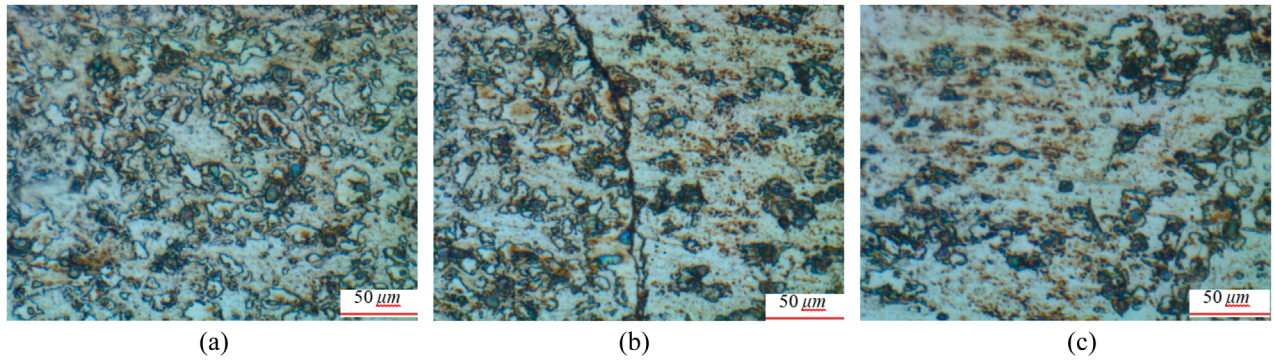

FIGURE 8
Microstructures of the X80 pipeline steel welded joint at different locations: **(a)** BM; **(b)** HAZ/WM interface; **(c)** Weld center.

Cracks 1 and 4 are situated within the BM and weld center, respectively, where material properties are relatively homogeneous. The crack-tip stress fields exhibit symmetrical distributions, with maximum von Mises stresses of approximately 885 MPa and 700 MPa, respectively (see Figures 12a,d).

Crack 2 is located in the HAZ, where the maximum crack-tip stress reaches about 845 MPa. Due to the gradual transition of material properties on both sides of the crack, the stress field shows only slight asymmetry (Figure 12b).

In contrast, Crack 3 is positioned at the BM/WM interface, where significant mechanical property differences exist across the crack flanks, resulting in a markedly asymmetric crack-tip stress distribution (Figure 12c). This observation indicates that material heterogeneity at the weld interface strongly influences the local crack-tip stress state, suggesting this region as a preferential site for hydrogen-induced crack initiation and growth (Wang et al., 2024c).

The distribution of equivalent plastic strain at the crack tip reflects the differences in mechanical properties and corresponding deformation characteristics across various regions of the welded joint, as shown in Figure 13. Crack 1, located in the BM region with relatively high yield strength, exhibits low plastic strain at the crack tip (maximum approximately 0.175), indicating low deformation concentration, stable crack propagation, and good resistance to plastic deformation, resulting in lower sensitivity to HIC. In contrast, Crack 2 in the HAZ shows slightly increased local plastic strain (maximum around 0.185) due to welding-induced thermal softening, despite good material continuity. The expanded plastic zone makes this region more susceptible to microdamage, thereby increasing the risk of HIC. Crack 3, positioned at the BM/WM interface where significant mechanical property gradients exist, exhibits the highest maximum plastic strain of 0.292. The pronounced plastic strain localization reflects severe softening and enhanced local deformation capacity at the interface, leading to plastic damage accumulation and marking this region as the most sensitive to HIC within the joint. Crack 4, located at the weld center, despite relatively uniform microstructure, shows lower strength and a maximum plastic strain of 0.283, indicating strong local plastic deformation capacity and a similarly high risk of HIC. Overall, the plastic strain distribution within the joint negatively correlates with material strength, and the high plastic deformation in softened regions is a key factor promoting preferential hydrogen-induced crack initiation and propagation.

The spatial variation of mechanical properties significantly influences the distribution of crack-tip mechanical fields, and heterogeneous mechanical responses can cause deviation in crack propagation paths. Under stable operating conditions, crack growth is primarily governed by the crack-tip opening stress. Considering that HIC typically occurs under constant or slowly varying loads,

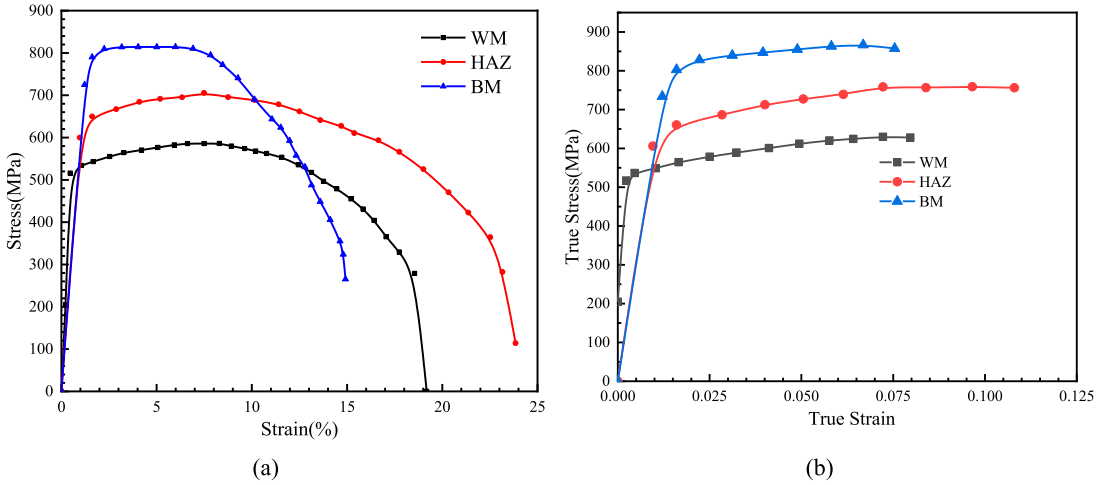

FIGURE 9
Stress–strain curves of the X80 welded joint **(a)** Engineering stress–strain curves and **(b)** True stress–strain.

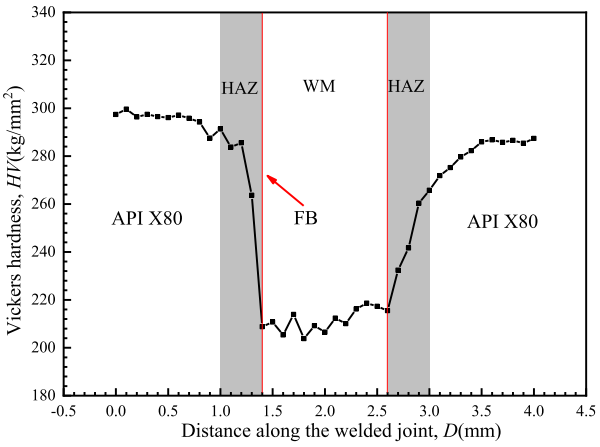

FIGURE 10
Hardness distribution along the X80 pipeline steel welded joint.

this study infers from the stress field evolution that cracks tend to propagate toward regions with higher yield strength.

To verify this hypothesis, the next section will present crack propagation path simulations for different initial cracks within the welded joint based on the USDFLD subroutine, aiming to thoroughly analyze crack deflection behavior and potential failure modes in heterogeneous structures.

4.4 Crack propagation paths at different locations of the welded joint

HIC is a delayed fracture phenomenon occurring in metallic materials under sustained tensile stress combined with high-pressure hydrogen environments. The constant external load and the localized stress field at the crack tip are the primary driving forces for HIC propagation. Under continuous stress, stress concentration in defect regions such as microcracks or heterogeneous microstructures may initiate crack nucleation and unstable growth. This section analyzes the influence mechanism of mechanical heterogeneity on HIC crack propagation paths from a mechanical perspective.

Based on crack location analysis, HIC cracks generally tend to propagate toward regions with higher yield strength. This is because high-strength areas exhibit lower toughness and reduced plastic dissipation capacity at the crack tip, thereby decreasing resistance to crack growth. Conversely, low-strength regions possess greater ductility and plasticity, which can partially relieve crack-tip stress concentration and enhance resistance to crack propagation. The crack propagation paths are shown in Figure 14. These findings highlight that gradients in material strength distribution are key factors influencing the deflection of hydrogen-induced crack paths.

4.5 Evolution of mechanical fields at the growing crack tip

In this section, a finite element model based on ABAQUS was developed to simulate crack propagation behavior at the weld interface region under constant load. The evolution of crack-tip mechanical fields during crack growth was analyzed by extracting von Mises stress and equivalent plastic strain (PEEQ) distributions at crack extensions of 200 μm, 400 μm, and 600 μm, as shown in Figure 15.

The results indicate significant changes in the stress and strain states near the crack tip as the crack advances. The mechanical field characteristics at the newly formed crack tip differ notably from those of the initial stationary crack. This variation mainly arises from local unloading ahead of the crack front during propagation, which releases and redistributes the original stress concentration, accompanied by a concurrent adjustment in the plastic zone size. Further observation of Figure 15 reveals pronounced residual stress

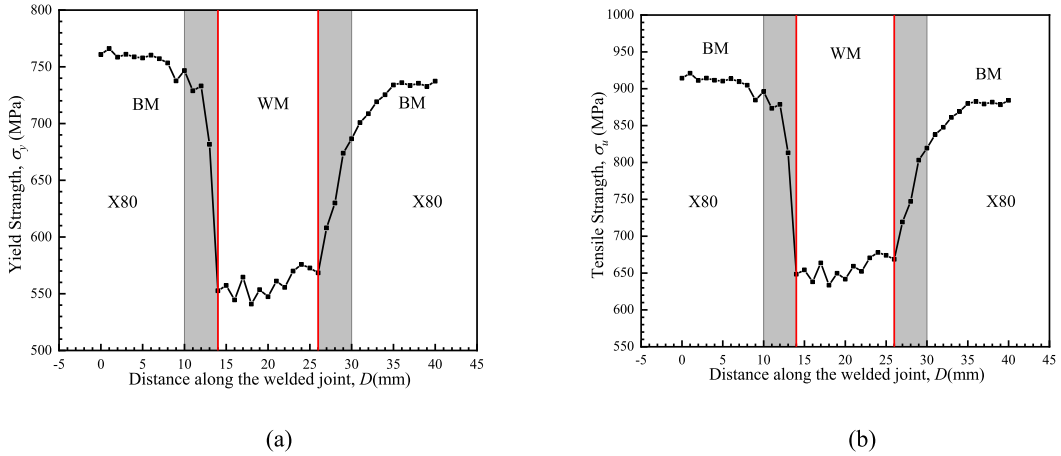

FIGURE 11
Strength distribution of the X80 pipeline steel welded joint: **(a)** Yield strength; **(b)** Tensile strength.

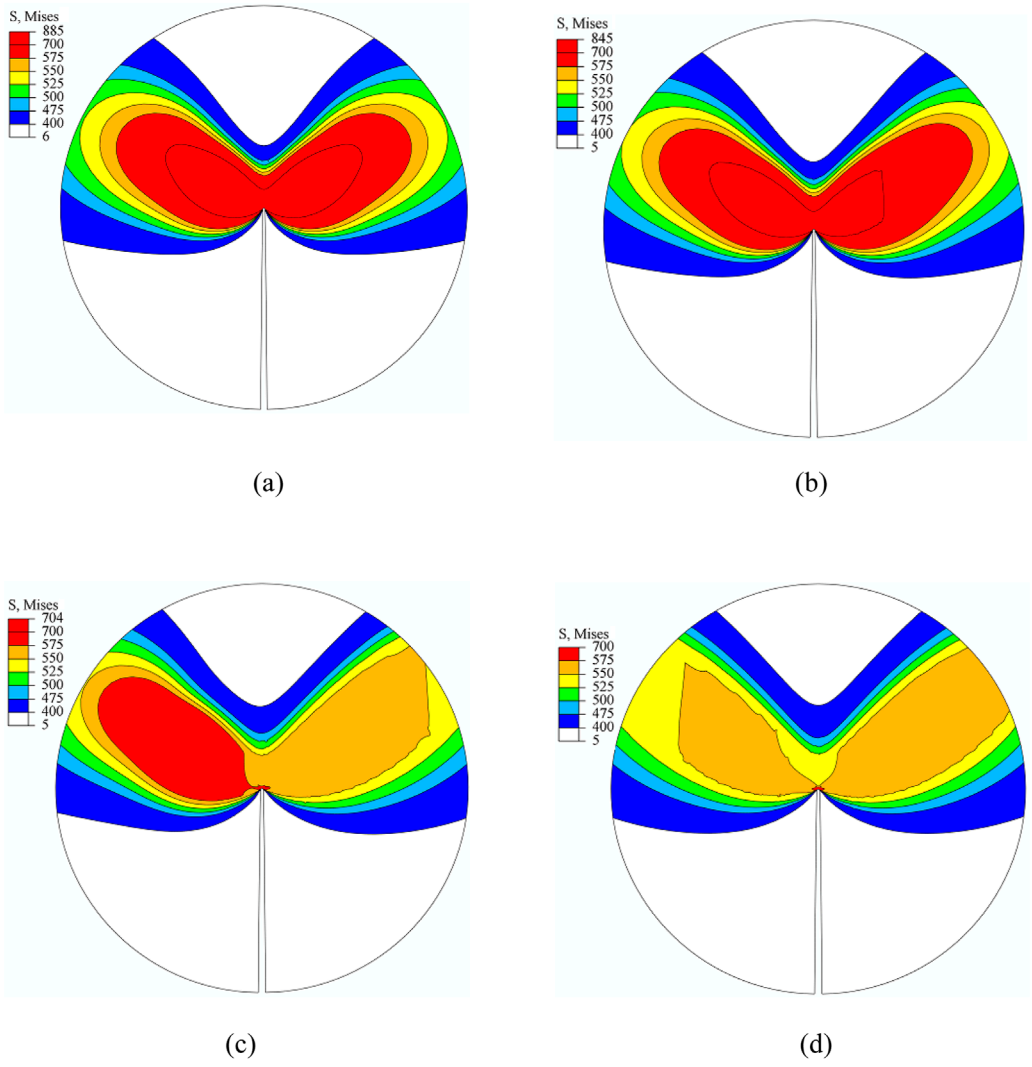

FIGURE 12
Distribution of crack-tip stress fields at different locations. **(a)** BM **(b)** HAZ **(c)** Interface **(d)** WM.

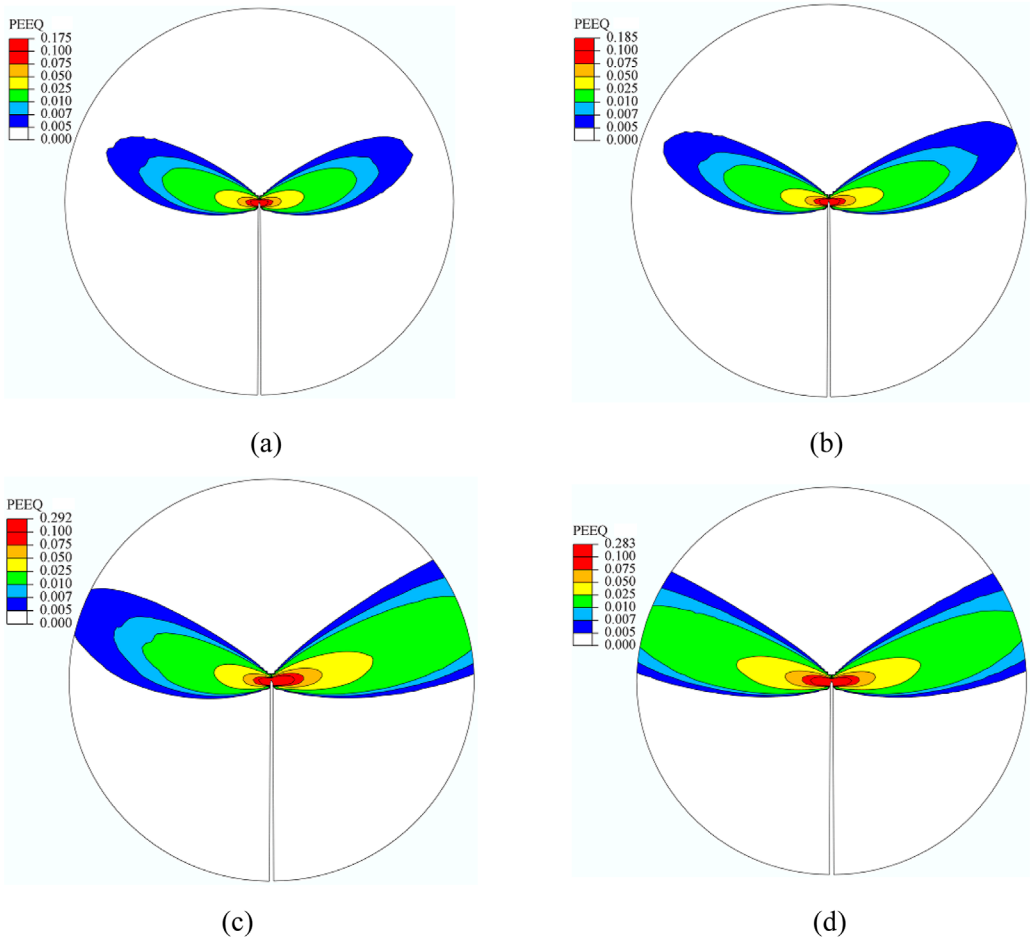

FIGURE 13
Distribution of crack-tip strain fields at different locations. **(a)** BM **(b)** HAZ **(c)** Interface **(d)** WM.

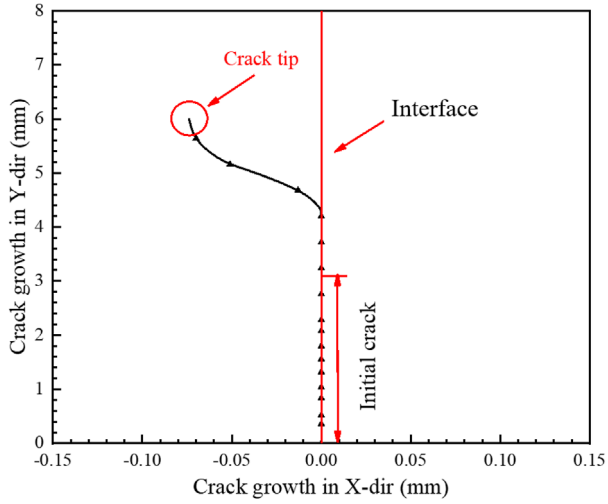

FIGURE 14
Crack propagation path and crack growth length at the DMWJ interface.

and plastic strain retention zones along the crack growth path. A local reloading zone forms near the new crack tip, while the crack wake retains a "plasticity memory zone" accumulated during previous growth stages. Although PEEQ values in the wake are slightly lower than those near the new tip, they remain elevated, indicating clear "transferability" and "history dependence" of the crack-tip response. Moreover, the mechanical field reconstruction induced by crack growth is mainly confined to the high-strain near-tip region, while stress states farther from the crack front remain essentially stable. This suggests that the propagation-induced disturbance to the overall stress distribution is localized.

In summary, under constant loading, crack growth triggers a localized mechanical field evolution centered on the crack-tip plastic zone, exhibiting spatial continuity and deformation inheritance. This plasticity-dominated evolution mechanism provides fundamental mechanical support for stable HIC propagation under non-instantaneous loading conditions. Although hydrogen diffusion and environmental corrosion effects are not explicitly considered here, the observed crack-tip evolution trends offer valuable insights into the driving mechanisms of HIC.

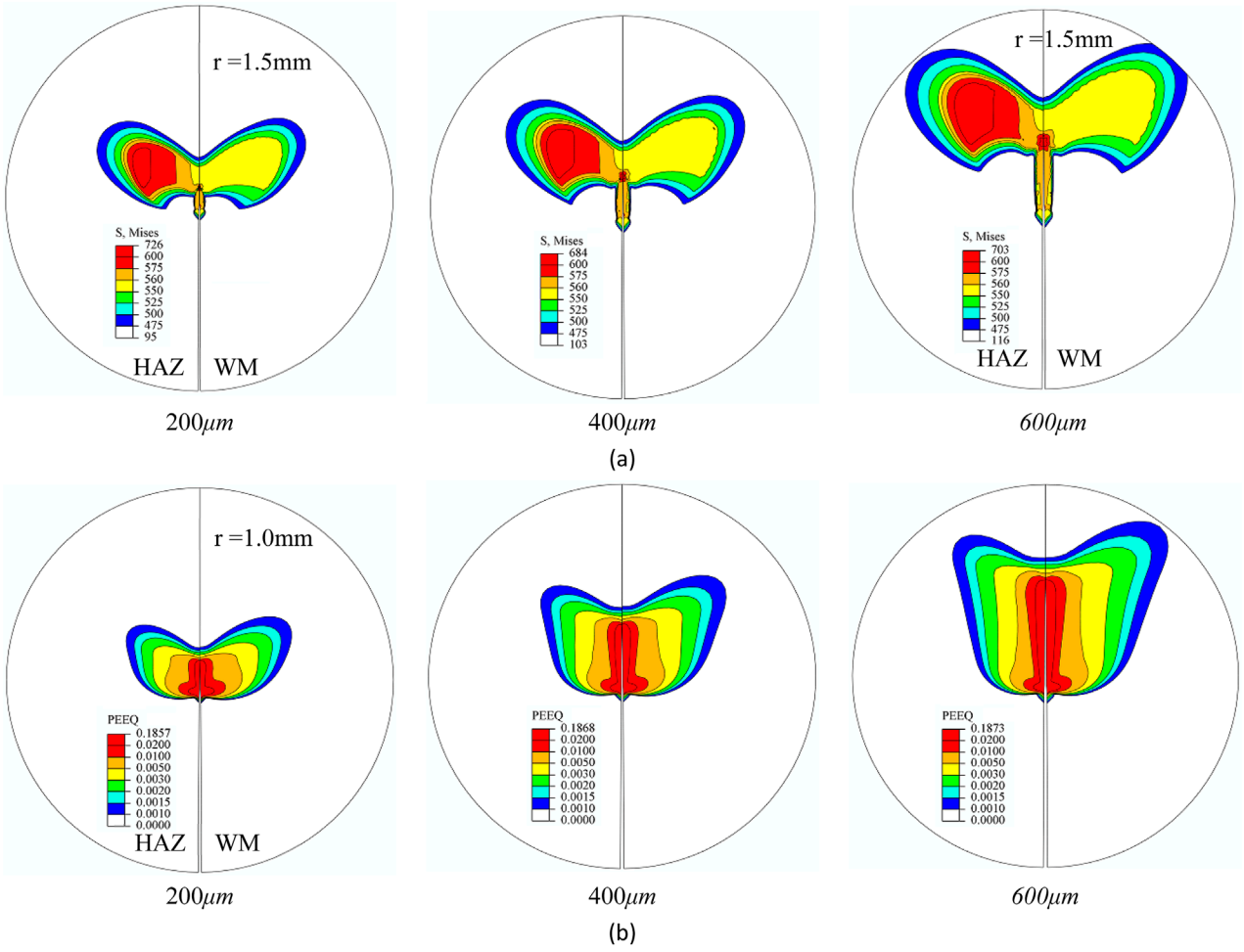

FIGURE 15
Mechanical fields at the growing crack tip near the weld interface: **(a)** Crack-tip von Mises stress; **(b)** Crack-tip equivalent plastic strain.

5 Conclusion

This study systematically analyzed and characterized the microstructure and local mechanical properties of X80 pipeline steel welded joints. A user-defined subroutine (USDFLD) was implemented to realize the continuous assignment of material properties within the finite element model, capturing mechanical heterogeneity. Crack propagation paths under HIC conditions were also investigated. The main conclusions are as follows.

1) The X80 BM primarily consists of polygonal ferrite and bainite. The HAZ exhibits significant recrystallization with increased and randomly distributed grain sizes. The weld center shows pronounced grain coarsening due to temperature gradients and cooling rate differences. Microstructural variations among different joint regions are the fundamental cause of spatial mechanical heterogeneity.
2) The welded joint exhibits a typical "V"-shaped hardness profile, with the highest hardness in the BM (~296 HV) and a marked decrease to around 209 HV in the HAZ. The overall hardness difference exceeds 80 HV, indicating a significant strength gradient. The hardness jump at the interface creates a pronounced stress concentration zone, making it a potential sensitive site for preferential HIC initiation.
3) Material property heterogeneity strongly affects the distribution of stress and plastic strain at the crack tip. The high-strength side tends to develop stress concentrations, while the low-strength side undergoes larger plastic deformation. The interface region, combining stress peaks and plastic strain localization, is identified as the most HIC-sensitive and weakest area in the welded joint.
4) Crack propagation paths generally tend to deviate toward regions with higher yield strength. These areas possess lower toughness and are less capable of alleviating crack-tip stress concentration, thereby reducing fracture resistance. Conversely, low-strength regions dissipate stress through plasticity mechanisms, enhancing resistance to crack growth and inhibiting HIC.
5) During crack propagation, the crack-tip von Mises stress and equivalent plastic strain undergo significant evolution. Local unloading at the advancing crack tip leads to stress and plastic zone reconfiguration, forming residual stress and "plasticity memory" zones along the crack path. The influence of crack

growth is mainly confined to the near-tip region, with limited impact on the far-field mechanical state, indicating a localized effect of crack extension.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

Author contributions

YJ: Data curation, Investigation, Methodology, Validation, Writing – original draft, Writing – review and editing. HX: Investigation, Methodology, Project administration, Resources, Writing – review and editing. ZW: Formal Analysis, Funding acquisition, Methodology, Validation, Writing – review and editing.

Funding

The author(s) declare that financial support was received for the research and/or publication of this article. Shaanxi Provincial Natural Science Basic Research Program (2025JC-YBMS-542), Key Scientific Research Program of Shaanxi Provincial Department of Education (24JR048), Xianyang Innovation Capability Support Program - Excellent Innovation Team Program (L2024-CXNLKJRCTD-KJTD-0009) and Scientific Research Projects of Shaanxi Energy Institute (2024KYTD05).

Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Generative AI statement

The author(s) declare that no Generative AI was used in the creation of this manuscript.

Publisher's note

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frontiers | Frontiers in Materials

TYPE Original Research
PUBLISHED 10 September 2025
DOI 10.3389/fmats.2025.1623918

OPEN ACCESS

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RECEIVED 06 May 2025
ACCEPTED 21 July 2025
PUBLISHED 10 September 2025

CITATION
Mei L, Wu R, Kang W, Cao Y and Li R (2025) Integrated approaches to selection control, microstructural analysis, and reliability assessment for bare dies.
Front. Mater. 12:1623918.
doi: 10.3389/fmats.2025.1623918

Integrated approaches to selection control, microstructural analysis, and reliability assessment for bare dies

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Due to limitations of device size and weight and the demand for multi-functional, high precision, and highly reliable devices, bare dies have been adopted instead of packaged components. By using dies directly without packaging, costs are somewhat reduced. However, without packaging protection, higher requirements on quality and reliability are imposed on bare dies. Based on system reliability, a comprehensive assessment must be made based on factors such as selection control, structural management, functional performance, and environmental adaptability. A typical die was initially selected, based on the application reliability risk analysis for bare dies, reliability evaluation projects were designed, and the reliability evaluation scheme was confirmed. The functionality, performance, reliability, and adaptability of the bare die were evaluated. The practical results demonstrated that the integrated evaluation method can effectively avoid the use of components with quality risks or insufficient reliability, contributing to the goal of reducing costs while ensuring product quality and reliability.

KEYWORDS

bare die, integrated approaches, application reliability, selection control, risk analysis

1 Introduction

With the development of equipment for high precision, high reliability, long life, and deep space applications (Whelan et al., 2001; Zheng et al., 2013; Scheffer, 2016), there has been an increasing demand on the functionality, performance, integration density, and reliability of integrated circuits under constraints of equipment size and weight. This trend had led to the growing widespread application of bare dies. Therefore, it is crucial to not overlook evaluation of the quality and reliability of newly selected bare dies.

Through the known-good bare die (KGD) technique (Singh et al., 1997; Chen et al., 2022; Yoo and Meng, 2021), reliability tests such as functionality, performance, burn-in, and screening can ensure the quality and reliability of bare dies. The series standards that have been established include American JESD49 KGD (Procurement Standard for Semiconductor Die, 2020), Japanese EIAJ EDR-4703, and European ES59008 and IEC62258. The entire process from design

verification to production process control and die screening assures the quality of bare dies.

To meet the equipment requirements for bare dies, it is necessary to conduct analysis of the selection management of bare dies based on system reliability. In order to respond to the demand for domestic bare dies and requirements for cost reduction and efficiency improvement, it is necessary to select products from mature, stable, and high-quality suppliers. Accordingly, in a typical application environment, the application's reliability must be scientifically, effectively, and efficiently assessed to support bare die application. Based on the risk analysis of the reliability of bare dies, the physical properties, function, performance, environmental adaptability, and assembly adaptability are evaluated to verify whether bare die reliability and quality are suitable for application. The main processes to selective control are shown in Figure 1. Based on the requirements of the project, we selected a typical one and verified the effectiveness of the system analysis method. Considering both the typical application environment of the equipment and a reliability risk analysis of the application, we developed an evaluation plan for initial selected. This plan aimed to assess various aspects of the die, including physical characteristics, functionality, performance, environmental adaptability, and assembly compatibility in order to evaluate the suitability of the typical die.

2 Selection control method for bare dies

To ensure that a selected bare die can be reliably applied in equipment, equipment requirements must be obtained for its typical application environment (Luo et al., 2001), functional performance, physical characteristics (Giannakaki and Katsanidis, 2023), and acceptable failure rate of bare dies. To meet the quality and reliability requirements of the equipment when choosing typical bare dies (Zieja et al., 2018; Kimmerle and Avenhaus, 2023), both the product supplier (Gheidar-Kheljani and Halat, 2024) and typical products should both be evaluated.

The reliability of components depends on the production process (Samokhin et al., 2019) and the management level of suppliers (Deviatko et al., 2024). To ensure the consistency, stability, and traceability of components, the capability assessment of suppliers (Allenbacher and Berg, 2023; Chen et al., 2020; Hulevich and Nalivaiko, 2021) includes design, raw material management, product process control (Hidayat et al., 2019;

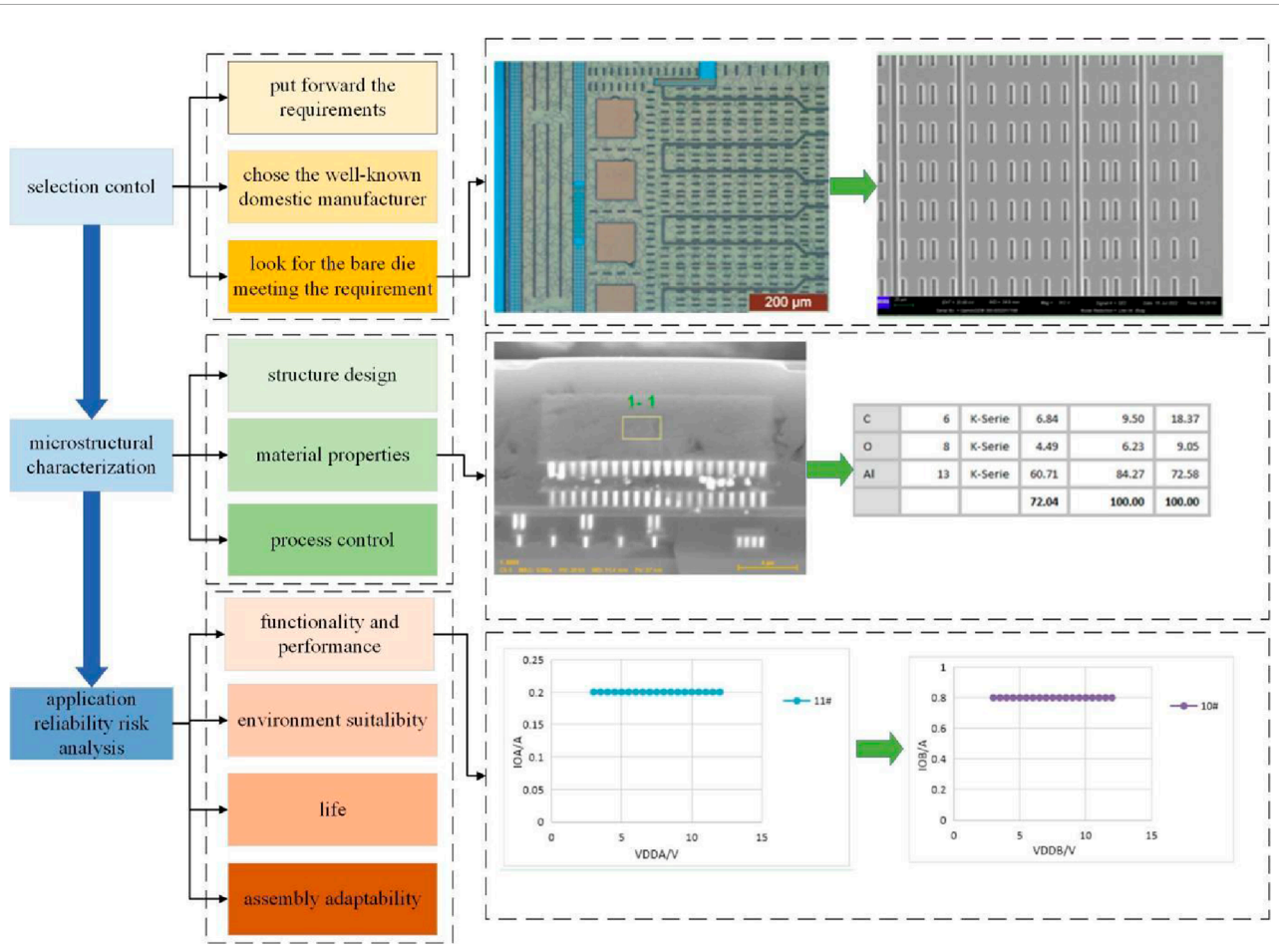

FIGURE 1
Schematic diagram of the method for systematically evaluating bare dies.

TABLE 1 Structural units of bare die X43XXX.

Structural unit	Structural evaluation element
Die	Appearance quality
	Boundary dimension
	Die layout and technology
	Die profile structure
Pad	Pad dimension
	Pad composition
Passivation layer	Passivation layer integrity

TABLE 2 Structural analysis test items.

Test item	Test method
Physical scale	Domestic manual and MIL-STD-883 method 2016
Internal visual inspection	MIL-STD-883 method 2010
Glass passivation layer integrity	MIL-STD-883 method 2021
Sample preparation	—
Scanning microscope observation and energy spectrum analysis	MIL-STD-883 method 2018

Mayrhofer et al., 2020; Sunadi et al., 2020), non-conforming product handling, stable supply (Spekman et al., 2001), and quality management (Kwilinski et al., 2023).

When selecting a typical die, products from well-known domestic manufacturers with established processes should be preferred. The manufacturer should be chosen from the top of the industry which reliably produces proven products.

After investigation, the typical power management bare die X43XXX was selected to apply in a specific device. The die had passed the qualification test as required and had stable supply. The evaluation of the selected typical products included microstructural characteristics, function and performance, environmental adaptability, and assembly adaptability.

3 Microstructural analysis for bare dies

Unreasonable structural design, mismatched material properties, or unstable process control may lead to a decline in the inherent reliability of components and increase potential safety hazards (Deviatko et al., 2024; Akbari et al., 2021). The physical properties of a bare die to be evaluated will affect its inherent reliability, operational reliability (Cheng et al., 2022; Feng et al., 2021), and service life (Alekseeva et al., 2023). It is necessary to analyze whether structural design, materials, and processes meet the requirements of the special application environment of the equipment. Structural analysis can determine the physical characteristics of potential operational reliability risks and eliminate them before the die is applied.

Microstructural characteristics (such as structure, process, and material) significantly influence the life expectancy and reliability of bare dies, necessitating thorough evaluation. Structural analysis is crucial in reliability assessment as it effectively identifies components with prohibited or restricted structures, as well as those posing quality risks, from being integrated into equipment. Structural analysis gives insights into the actual composition of electronic components and uncovers potential design weaknesses and manufacturing flaws, thereby ensuring compliance with established standards.

We decomposed the structural units of a typical bare die and identified key elements. The structural units and evaluation factors of the X43XXX die are listed in Table 1, including the die itself, bonding pads, and passivation layers. After decomposing the structural units, performance analysis and calculation of these units along with their constituent materials must be conducted. Based on the structural evaluation criteria for the bare die, structural analysis tests were formulated. The structural analysis test items for the X43XXX structure are shown in Table 2.

Three samples were selected for structural analysis. First, their physical dimensions were measured and subject to internal visual inspection using a stereo microscope and a metallographic microscope. The dicing quality of bare die X43XXX was good, with no observed damage or cracks. The surface showed no signs of blistering, peeling, or erosion. The backside was a substrate layer, and there were no metalized coatings on its surface. The passivation layer integrity of the die was qualified.

After embedding the bare die sample and performing cross-section inspections, a scanning electron microscope (SEM) and energy-dispersive spectrometer were utilized to analyze the structure and materials of the dare die. This revealed that the die featured a layered architecture encompassing surface passivation layers, internal multilayer metallization, interlayer bare dielectrics, and a bottom substrate layer. Further analysis indicated that the die's substrate was composed of silicon (Si), with aluminum (Al) as the primary constituent in its metallization layers. The thickness of the topmost metallization layer was measured to be approximately 5.5 μm. The intermediate bare dielectric layers were found to primarily consist of carbon (C), oxygen (O), aluminum (Al), and silicon (Si). Additionally, the vias within the die were predominantly composed of carbon (C), oxygen (O), aluminum (Al), tungsten (W), and titanium (Ti).

By examining the die using a metallographic and a scanning electron microscope, it was observed that the bonding pad surface in the bonding area was smooth and continuous, with no signs of peeling, flaking, or bulging. It can be concluded from the structure, raw materials, and process design that the bare die had a reasonable structural design and contained no prohibited or restricted processes or materials. Therefore, this die met the requirements for encapsulation.

4 Application reliability risk analysis for bare dies

4.1 Functionality and performance for bare dies

To assess the technical specifications of the equipment, we conducted a baseline evaluation of functionality, performance, key parameter characteristics, power voltage limiting value, and operating temperature limiting value for the typical bare die. This was to verify whether the actual performance metrics of the bare die cover the specified range for the product. Baseline testing of key parameter characteristic curves can be used to help designers understand parameter variation patterns and take protective measures when necessary. Furthermore, baseline testing of the operating temperature limiting value can reveal the typical temperature application range of the bare die to prevent designers from overstepping this range, which could lead to die failure.

Static, functional, and switching tests were conducted according to the specifications on this bare die at three temperature points (−55°C, 25°C, and 125°C). All test results were satisfactory.

Based on the equipment application design analysis and the recommended operating conditions in the detailed specifications, the static current of the die under different input voltages and temperatures was fitted to understand the characteristic curves of the die. Two samples, 10# and 11#, were selected for testing. Under the power supply of A line VDDA ranging from 3 V to 12 V, the trend of the static current output current of A line IOA was measured; B line was similarly measured.

Within a temperature range of −55°C to 125°C with a temperature step interval of 25°C, tests were conducted on IOA and IOB. After the experiments, parameter fitting was performed. No abnormal phenomena were observed in the die during the testing process.

4.2 Environmental suitability of bare dies

Typical environments include temperature (Wang et al., 2024) and the mechanical environment. Components used in equipment should be able to withstand temperature environmental stress during storage, transportation, launch, ascent, and operation. The temperature factors that have a significant impact on components include high temperature (Caria et al., 2024) and low temperature and temperature variation (Rathaur et al., 2024). High temperatures (Rathaur et al., 2024; Wang Jianqiang et al., 2023; Tayyab et al., 2022) may lead to changes in parameters such as power factor and dielectric constant. Temperature-related evaluation tests include temperature cycling (Teverovsky, 2007; Boldyrjew-Mast et al., 2020), thermal shock (Zhong et al., 2024; Wang Liujue et al., 2023; Zhou et al., 2022), high-temperature storage tests (Wang et al., 2020; Jiang et al., 2024), and power temperature cycling tests (Boldyrjew-Mast et al., 2020; Vankayalapati et al., 2024). The evaluation test items and conditions were confirmed based on the temperature environment that the components had experienced, and the thermal environment adaptability of the components in practical applications was evaluated (Chen and Huang, 2009).

The environmental adaptability of bare dies is related to the operation stage of the equipment. Factors with a significant impact on bare dies include high temperatures, low temperatures, and thermal cycling.

Temperature cycling tests can be used to evaluate the ability of a die to withstand alternating extreme high and low temperatures and to analyze the effects of such temperature changes on the die; before its first selection, the anti-static capability of a bare die should be assessed. To verify the quality or reliability of bare dies under specified conditions, life testing can be employed to determine their life limit (Srivastava and Agarwal, 2024). Other special environments must be identified based on the typical operating environment of the equipment (Pan, 2024; Singh and Kalra, 2023), such as mechanical stress, salt fog, humidity, and space radiation. When bare dies are applied, it is essential to consider their compatibility with packaging technologies.

By conducting life tests on the products, the failure rate and mean time between failures (MTBF) of the products are obtained based on the corresponding calculation model (Leong et al., 2025; Fang et al., 2023). For instance, the failure rate of the product was estimated using the chi-square stepwise method, and the MTBF of the product was obtained by taking its reciprocal. The failure rate λ,r represents the number of failures; $X_{\alpha}^{2}(2r+2)$ is the chi-square distribution value under the confidence coefficient 1-α. The calculation model is

$$\lambda = \frac{x_{\alpha}2(2r+2)}{2 \times N \times H}. \tag{1}$$

Based on when the methods were proposed, acceleration models can be classified as physical, empirical, or statistical. The physical acceleration model was proposed based on the chemical explanation for product failure. A typical physical acceleration model is the Arrhenius model (Youn et al., 2024; Xing and Yang, 2023), which describes the relationship between product life and temperature stress. The Arrhenius model (Yuan et al., 2024) is often used in engineering for the accelerated life model under temperature stress:

$$\xi = Ae^{\frac{E}{KT}}, \tag{2}$$

where ξ represents the pseudo-lifetime following the distribution or the coefficients of the degradation model in which the characteristic values of the degradation amount conform, A is a constant, E is the activation energy and is related to the material, K is the Boltzmann constant, and T is the absolute temperature. The logarithm of both sides of the expression is

$$\ln\xi = a + b/T. \tag{3}$$

Among them, a = InA, B = E/K.

We selected four samples for steady-state life tests. After 1,000 h, no significant abnormalities were observed in the die appearance, and the die testing was qualified; two samples were selected for temperature cycling tests. After the test, no significant abnormalities were observed in the die appearance, and the die testing was qualified. According to the specifications of this bare die, its electrostatic discharge sensitivity level was 1°C. Two samples were selected, and an ESD (HBM) voltage of 1000 V was applied to the bare die for testing. During the test, there were no abnormalities in the die, and it passed the 1000 V screening test with qualified results.

TABLE 3 Tensile failure values of gold wire for four samples (unit: gf).

1#	2#	3#	4#
7.497	6.281	7.758	8.010
5.803	7.219	8.920	7.410
10.240	9.411	6.919	9.697
9.747	8.709	7.490	9.041
7.239	8.323	7.945	7.681
7.250	8.953	8.691	9.169
5.668	6.513	9.428	7.994
8.018	8.759	9.717	8.973
6.814	8.362	8.864	8.973
6.005	10.272	10.628	11.173
7.902	10.117	10.377	13.470
8.818	8.882	11.327	8.275
9.578	10.240	12.069	8.236
7.497	6.281	7.758	8.010
5.803	7.219	8.920	7.410
10.240	9.411	6.919	9.697
9.747	8.709	7.490	9.041
7.239	8.323	7.945	7.681

The equipment components had to be subject to such mechanical environmental stresses as impact, vibration, and acceleration for the stages of transportation, launch, operation, and return. Components may generate electrical noise, electrical parameter drift, or other abnormal parameter phenomena in a vibrating environment. Mechanics-related tests include sweep frequency vibration (Sang and Zhang, 2020), mechanical shock, centrifugal tests, and vibration fatigue (Barraza-Contreras et al., 2023). Based on the mechanical environment confirmation and evaluation test items and conditions that the components experienced, we evaluated the mechanical environment adaptability of the components in practical applications (Dang et al., 2025).

4.3 Assembly adaptability for bare dies

To investigate the adaptability of typical assembly processes for the bare die, it was assembled according to typical application methods. After assembly, the bonding strength and die shear force were evaluated. Simultaneously, environmental adaptability after assembly, such as temperature and mechanical conditions, were verified through tests like thermal cycling and vibration to ensure reliability.

To analyze the application environment of the bare die, a typical multilayer mixed-pressure board was used as the circuit substrate. After cleaning and drying the substrate, the bare die was cured in an oven at 150°C. Post-curing, the substrate was placed on the heated platform of appropriate equipment for gold wire bonding.

After the bonding process, the substrate was placed on the worktable of a push–pull force tester. The gold wire pull strength of the die was measured first, followed by the push–pull force test of the die. The failure values of the 25-μm-diameter gold wire pull strength for the four samples are shown in Table 3; the minimum failure value of the gold wire pull strength was 5.668°gf, meeting the requirement for the minimum pull force failure value (3.0°gf).

In the die thrust test, the minimum failure thrust value was 9.817 kg. The die was 2141 μm × 1610 μm in size, covered an area of 3.45 mm^2, and satisfied the shear strength requirements.

Following typical assembly, the bare die successfully underwent temperature cycling, random vibration, and shock tests, with the system operating normally and all performance metrics adhering to design specifications.

5 Summary

Based on the demand for high reliability, high performance, low cost, and short equipment cycle, the application of bare dies has become a new focus. Based on the selection control and reliability risk analysis of bare die applications, a reliability evaluation plan was needed before using a bare die for the first time. The evaluation tests assessed the functions, performance, reliability, and environmental adaptability of the dies, ensuring quality control when selecting a bare die for equipment. Before installing and applying bare dies on equipment, it is essential to implement quality control over their design and manufacturing processes to ensure inherent reliability. A first-time application should be combined with typical equipment for reliability evaluation. After additional selection and other quality assurance measures, trial applications can be conducted. Post-installation, the equipment will undergo environmental testing. During this process, further analysis will be required to understand the degradation of bare die packaging.

Data availability statement

The original contributions presented in the study are included in the article/supplementary materia, further inquiries can be directed to the corresponding authors.

Author contributions

LM: writing – original draft, writing – review and editing. RW: writing – original draft, writing – review and editing.

WK: writing – review and editing. YC: writing – review and editing. RL: writing – review and editing.

Funding

The author(s) declare that no financial support was received for the research and/or publication of this article.

Conflict of interest

Authors LM, RW, WK, YC, and RL were employed by China Aerospace Science and Industry Corp.

Generative AI statement

The author(s) declare that no Generative AI was used in the creation of this manuscript.

Publisher's note

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