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Atomic layer deposited $HfZrO_4$-based memristive devices: annealing effect and multilevel storage capability

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In this work, an atomic layer deposited (ALD) $Hf_1Zr_1O_4$ (HZO)-based switching layer is investigated in the device structure of a TiN/HZO/TiN. The thickness of the switching layer is ~10 nm, which was grown by the thermal ALD at 250 °C by a super-cycle approach. Both pristine and annealed (400 °C for 60 s in N_2) devices exhibit stable bipolar resistive switching responses after an essential electroforming process. However, the annealed devices require a relatively higher forming voltage but significantly improved ON/OFF ratio than pristine devices, which can be due to a certain modification at the TiN/HZO interface. The significant improvement in the ON/OFF ratio is attributed to the formation of nano-crystallinity in the film and an increment in sub-oxide content. The X-ray photoelectron spectroscopy (XPS) analysis also reveals the formation of a significant amount of sub-oxide (HfO_{2-x} and ZrO_{2-x}) after the annealing process. Additionally, the pristine devices exhibit comparatively poor switching stability and show a systematic decrement in the hysteresis loop, i.e., 73% after 100 switching cycles, whereas only a ~22% drop is observed with annealed samples that significantly enhance the device stability. Lastly, the annealed device exhibits high volatility towards multiple programmable states, which can be useful in the development of multilevel memory storage, in-memory computation, and neuromorphic computation.

KEYWORDS
annealing effect, atomic layer deposition, ferroelectric memristor, HfZrO4, resistive switching

1 Introduction

The concept of memristor, or resistive random-access memory (ReRAM) technology, is undergoing a reappreciation as a possible solution to the hardware constrain for future computing. It is mainly propelled by the growth in artificial intelligence and machine learning based data analysis, which will benefit from switching to the in-memory computing architecture (Batra et al., 2018; Sebastian et al., 2020; Verma et al., 2019; Mehonic et al., 2020). Generally, in the memristive (or ReRAM) devices, a layer of transition metal oxide is sandwiched between two metal/conducting electrodes, and the switching phenomena happen by the movement of ions, vacancies, or metal atoms forming a pathway for the current flow between the top and bottom electrode (Wong et al., 2012; Zahoor et al., 2020; Zahoor et al., 2023). Among transition metal oxides, Hf-based monolayer and bilayer oxides

are extensively studied owing to their good control over the switching resistance and high compatibility towards complementary metal-oxide-semiconductor (CMOS) process (Napolean et al., 2022; Das and Khan, 2021). Moreover, HfO_2 also exhibits a high dielectric constant, which is beneficial for both logic and charge trap memories (Mulaosmanovic et al., 2020), and shows ferroelectricity/antiferroelectricity characteristics that can be made use of for the high-density memories and synaptic devices (Das and Khan, 2021; Mulaosmanovic et al., 2020; Covi et al., 2016; Lee et al., 2023; Park et al., 2015).

Tuning the resistive switching characteristic of HfO_2 by doping with metal ions is also extensively investigated, as Hf-based composites are reported to show unique performance as ReRAM devices (Napolean et al., 2022). Hf-based oxides are also excellent candidates for ferroelectric memory devices (FeRAM) (Lee et al., 2023; Park et al., 2015; Silva et al., 2023). Among various Hf-based multi-metal oxides, $Hf_xZr_{1-x}O_2$ is a unique material due to its very high ferroelectric performance, which depends on the amount of Zr, and this composite is reported to show a wide range of magneto-electric properties from purely dielectric to ferroelectric and to antiferroelectric characteristics (Silva et al., 2023; Park et al., 2017; Shibayama et al., 2018; Goh et al., 2020; Park et al., 2018; Park et al., 2019). Typically, a composition close to $Hf_{0.5}Zr_{0.5}O_2$ shows the maximum ferroelectric polarization (Silva et al., 2023; Park et al., 2017; Shibayama et al., 2018; Goh et al., 2020; Park et al., 2018; Park et al., 2019). The occurrence of ferro/antiferroelectricity in $Hf_xZr_{1-x}O_2$ has been extensively studied and is attributed to the formation of a metastable orthorhombic phase, whereas stable monoclinic and tetragonal crystal structures typically display dielectric or antiferroelectric nature (Silva et al., 2023; Park et al., 2017; Shibayama et al., 2018; Goh et al., 2020; Park et al., 2018; Park et al., 2019). In general, the formation of metastable orthorhombic phase happens at a temperature close to 600 ˚C and is influenced by the crystallite size, thickness, and the compressive strain in the $Hf_xZr_{1-x}O_2$ film (Silva et al., 2023; Park et al., 2017; Shibayama et al., 2018; Goh et al., 2020; Park et al., 2018; Park et al., 2019). The $Hf_xZr_{1-x}O_2$-based FeRAM needs very high temperatures to achieve its ferroelectric phase. But CMOS and ReRAM processes are unable to handle such high temperatures, and due to this mismatch, it becomes difficult to scale and integrate FeRAM into regular CMOS fabrication. The ferroelectric characteristics and FeRAM device performance of $Hf_xZr_{1-x}O_2$ devices are already reported in the literature as discussed above, but the detailed investigation of the memristive/ReRAM performance of Hf-Zr-based composites has not been explored yet. Ryu et al. (2014) reported the Zr doping of HfO_2, which enhances the resistive switching of HfO_2.

Herein, the resistive switching characteristics of ALD-grown $Hf_1Zr_1O_4$ are investigated. This work also explores the impact of the post-deposition annealing temperature (at 400 ˚C) on the memristive device performance, which significantly improves the device performance in terms of longer cyclic stability by enhancing the ON/OFF ratio. Additionally, a detailed material characterization including atomic force microscopy (AFM) to analyze the surface roughness, X-ray diffraction (XRD) for the deposited material phase, and X-ray photoelectron spectroscopy (XPS) to investigate the composition and sub-oxide formation. Furthermore, stability during potential cycling, retention, and programmability of the memristive devices are also investigated.

2 Memristive device fabrication

To fabricate a TiN/HZO/TiN device structure, a standard CMOS fabrication process was used in a cleanroom environment. A 50 nm thick TiN bottom electrode (BE) was deposited by reactive gas sputtering (Angstrom instrument) on a thermally grown SiO_2 (200 nm)/Si substrate in a conventional lift-off process, and the BE was patterned using a direct write lithography (Durham Magneto-Optics). Further, a 10 nm thickness of $Hf_1Zr_1O_4$ (HZO) layer was deposited by utilizing thermal atomic layer deposition (Veeco Fiji) at 250 ˚C using tetrakis dimethylamido hafnium IV(TDMAHf), tetrakis(dimethylamido)zirconium IV (TDMAZr), and H_2O, as hafnium, zirconium, and oxygen source, respectively. The ratio of Hf/Zr in the composite is maintained close to 1:1 by setting the ALD cycle number for HfO_2 and ZrO_2 to 1-1 in an ALD super-cycle sequence. Reactive ion etching (RIE) was used to, etch the dielectric layer, employing a 50:50 CHF_3/Ar mixture, after patterning with lithography to open the contact pads for the BE. This was followed by DC sputtering to deposit a 5 nm platinum capping layer over the BE pads. Finally, the top electrode (TE) was made by sputtering with 50 nm TiN and 5 nm Pt. The devices were annealed in a normal furnace at 400 ˚C for 60 s in a nitrogen atmosphere with a heating ramp rate of 5 ˚C per minute. The pristine devices are abbreviated as $HfZrO_4$-PR (HZO-PR), and annealed devices as $HfZrO_4$-AN (HZO-AN), respectively. The thickness of the HZO was measured by spectroscopic ellipsometry (JWA Wollam) during real-time deposition on a Si substrate with native oxide. The phase and crystalline nature of the samples were determined by grazing-incident X-ray diffraction (XRD), and the material composition in the deposited thin film was determined using X-ray photoelectron spectroscopy (XPS, Thermo-scientific Nexsa G2). The wide range survey spectra were taken with an X-ray pass energy of 50 eV, whereas high-resolution elemental spectra were acquired at a pass energy of 10 eV. The spectra were taken after 20-s Ar ion etching (cluster ion etching source) to remove surface contaminations. The XPS spectra were fitted with a CM line shape and Sherly background using CasaXPS software. Additionally, XPS depth profile analysis was also performed on selected dummy stacks of TiN/HZO/TiN devices before and after the annealing step to investigate the change in the HZO/TiN interface. The electrical measurement was carried out using a custom-built electrical board from ArC Instruments Ltd. (ArC ONE). All the measurements were carried out at room temperature by applying a voltage to the TE while the BE is kept grounded. The effective area of the device was (20 × 20) μm^2. Supplementary Figure S1 (see supporting information) shows the optical microscope images of the HZO-PR (see Supplementary Figure S1a) and HZO-AN (see Supplementary Figure S1b) with a schematic of the fabricated devices (see Supplementary Figure S1c).

3 Results and discussions

3.1 Material characterizations of HZO devices

Figures 1a,b show the AFM images of the as-deposited and annealed HZO film on SiO_2/Si substrate. The image in Figure 1b indicates a surface smoothening after the annealing step; apart from

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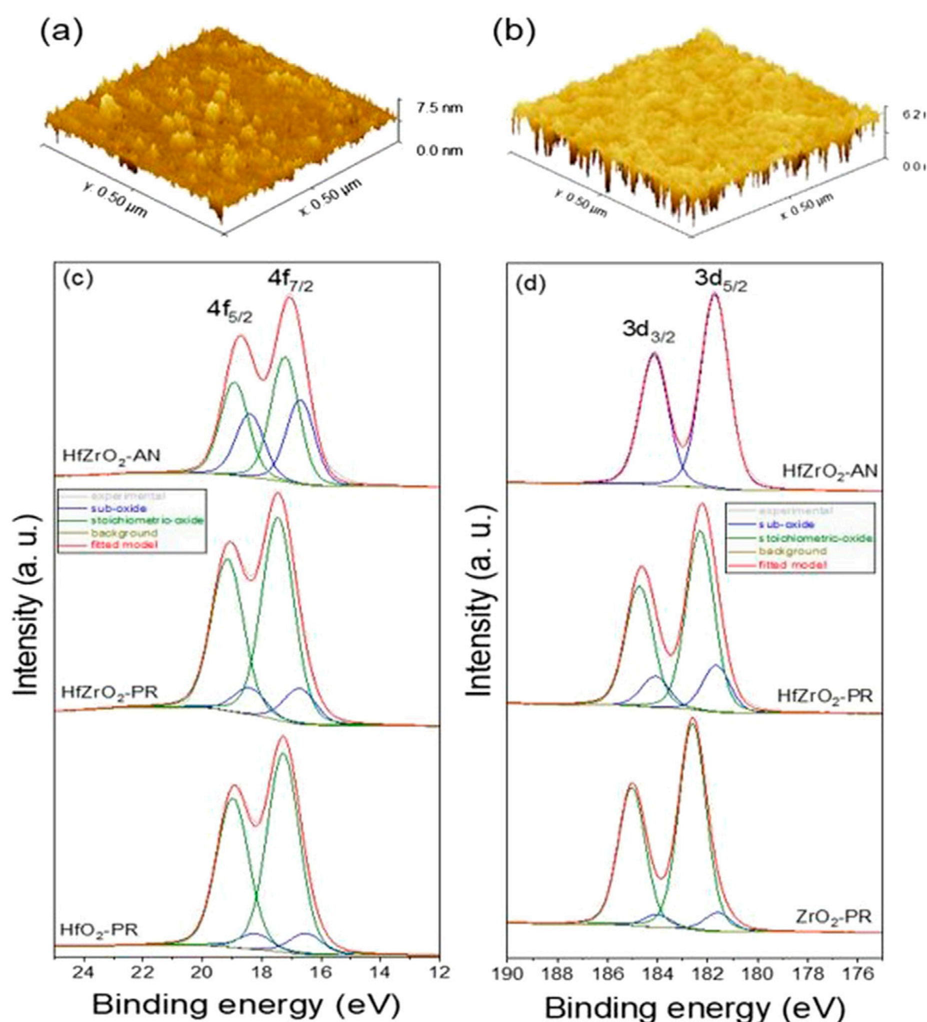

FIGURE 1
AFM image of **(a)** HZO-PR, and **(b)** HZO-AN thin film grown on SiO2/Si substrate, **(c)** Hf 4f, and **(d)** Zr 3d XPS spectra of HZO-PR, and HZO-AN thin film.

that, no apparent changes could be seen, like the film before and after the annealing process. Figure 1c shows the Hf 4f XPS spectra from HZO-PR and HZO-AN films grown on SiO_2/Si substrate. For comparison, XPS spectra of ALD-grown HfO_2 (Thermal ALD at 250 ˚C) are also included in Figure 1c (Puente et al., 2022; Sokolov et al., 2018; Triyoso et al., 2008). The hafnium sub-oxide (HfO_{2-x}) content in the pristine ALD HfO_2 and HZO-PR device is comparable; however, a significant increase in the HfO_{2-x} percentage is observed with HZO-AN. A similar trend in the sub-oxide content for zirconium oxide (ZrO_{2-x}) is evident in Figure 1d, where, after the annealing step, a complete transition into ZrO_{2-x} is observed. The peaks are compared with pristine ZrO_2 deposited with thermal ALD at 250 ˚C (Puente et al., 2022).

Additionally, Supplementary Figure S2 (see supporting information) shows the XRD profile from ALD ALD-deposited HZO layer (10 nm) on SiO_2 (200 nm)/Si substrate before and after the annealing step at 400 ˚C for 60 s. The as-deposited HZO layer is amorphous in nature, whereas heat-treatment at 400 ˚C (60 s) results in broad peaks centring at 2θ values of 35, 40, and 60, which infer the formation of nanocrystalline grains of a mixture of monoclinic, tetragonal, and orthorhombic phases of HfO_2, ZrO_2, and HZO.

3.2 Electrical characterization of HZO-PR and HZO-AN devices

The electrical measurement for the HZO-PR and HZO-AN is performed to evaluate the performance of the memristive devices (Serb et al., 2015; Stathopoulos et al., 2019). Both HZO-PR and HZO-AN devices require an initial electroforming process to achieve stable resistive switching responses. The electroforming process was done using the dedicated custom pulse generator sequence, in which a sequence of a set of 100 pulses with pulse widths ranging from 1 μs to 8 μs with a geometric progression and voltages ranging from 4.5 V to 9.5 V (depending on the device) with a 0.25 V step was applied on the devices. Inter-pulse duration was fixed at 10 ms. Two batches of devices (HZO-PR (5 devices) and

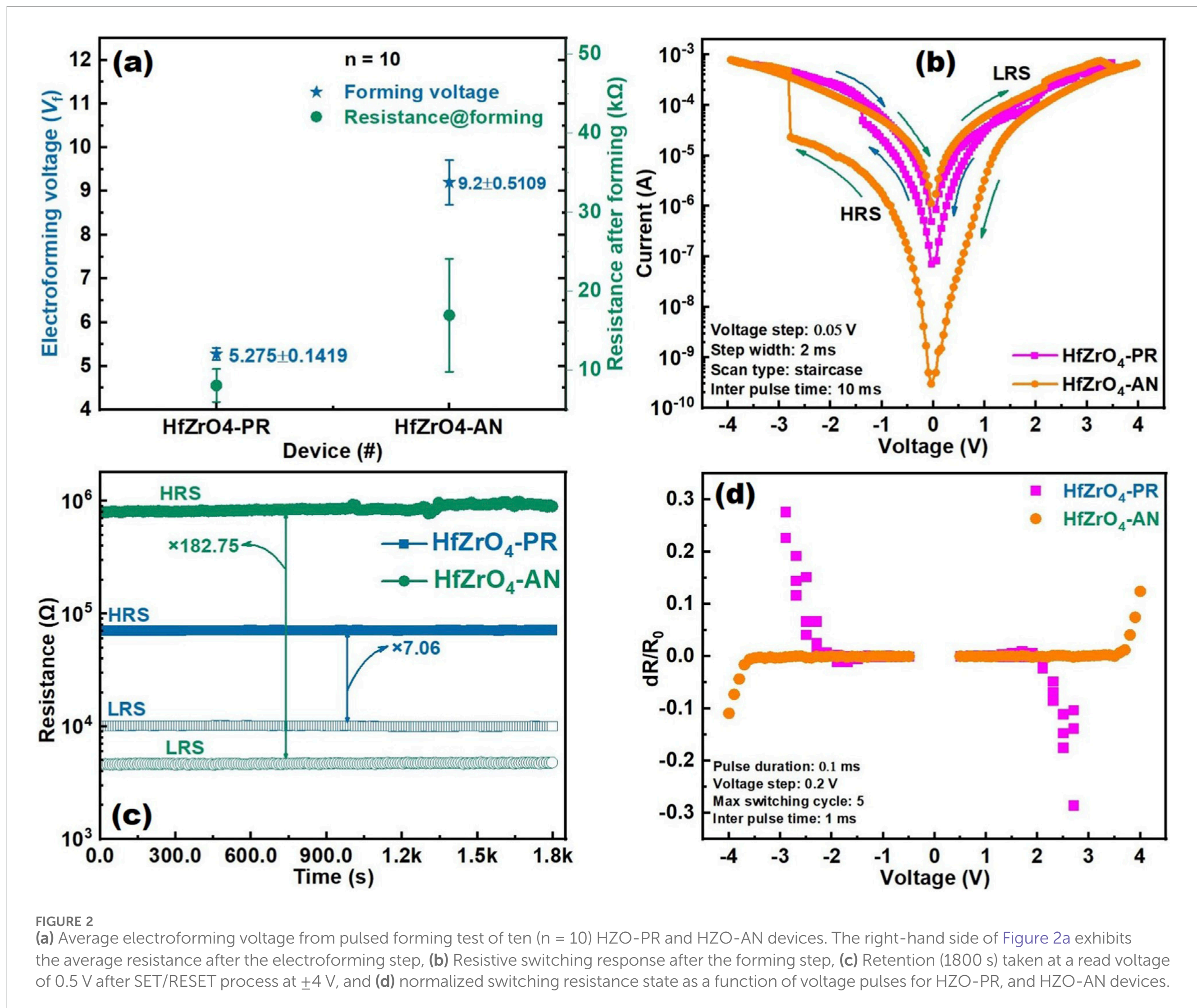

FIGURE 2
(a) Average electroforming voltage from pulsed forming test of ten (n = 10) HZO-PR and HZO-AN devices. The right-hand side of Figure 2a exhibits the average resistance after the electroforming step, **(b)** Resistive switching response after the forming step, **(c)** Retention (1800 s) taken at a read voltage of 0.5 V after SET/RESET process at ±4 V, and **(d)** normalized switching resistance state as a function of voltage pulses for HZO-PR, and HZO-AN devices.

HZO-AN (5 devices)) are evaluated, comprising a total of 10 devices, and an average value for electroforming voltage is determined. The mean forming voltage (V_f) for HZO-PR, HZO-AN, and the corresponding resistance after the forming step are shown in Figure 2a, and the forming process is shown in Supplementary Figure S3 (see supporting information). As observed, there is a clear difference between the forming voltage of HZO-PR and HZO-AN devices. The V_f for HZO-PR is ~5.3 V, and the forming voltage range is from 4.5 to 5.5 V. On the other hand, the V_f for HZO-AN is ~9.2 V (voltage range between 6.5 and 9.5 V). These outcomes seem to be in contrast to the earlier reported data (Swathia and Angappane, 2022). Generally, a reduction in the forming voltage with increasing deposition temperature is reported for ReRAM devices, and is attributed to the formation of a current path through the grain boundaries of the crystallized insulator layer (Swathia and Angappane, 2022). Hence, for the fabricated samples, the HZO/TiN interface might be altered during the annealing process. It is assumed that intermixing of metal cations (Ti, Hf, and Zr) and oxygen/nitrogen may have happened, resulting in the formation of a narrow, highly insulating interfacial layer between the HZO and TiN (Beckmann et al., 2019).

Figure 2b shows the resistive switching responses of the HZO-PR and HZO-AN devices after the initial forming process. The switching responses indicate an obvious distinction in the resistive switching characteristics of the HZO-PR and HZO-AN devices. The difference between the high resistance state (HRS) and low resistance state (LRS) is higher for HZO-AN devices when compared with the HZO-PR devices. Further, to inspect the long-term stability of the HRS and LRS set states, retention measurements are performed, and the obtained outcome is shown in Figure 2c, and the corresponding switching response taken before the retention is shown in Supplementary Figure S4a (see supporting information). The measurements are carried out at a SET/RESET voltage of ±4 V (SET and RESET *I-V* in the +Ve/-Ve direction taken before the retention step at 0.5 V), and for a duration of 30 min. In the case of HZO-PR, the ratio between HRS and LRS is approximately 7.06 times, whereas in the case of HZO-AN devices, this changed to approximately 182.75 times. A stable retention curve is observed for both HZO-PR and HZO-AN devices, confirming the stability of the HRS/LRS state formed at ±4 V.

To further investigate the difference in the switching behaviour, an analogue resistive switching parameter finder

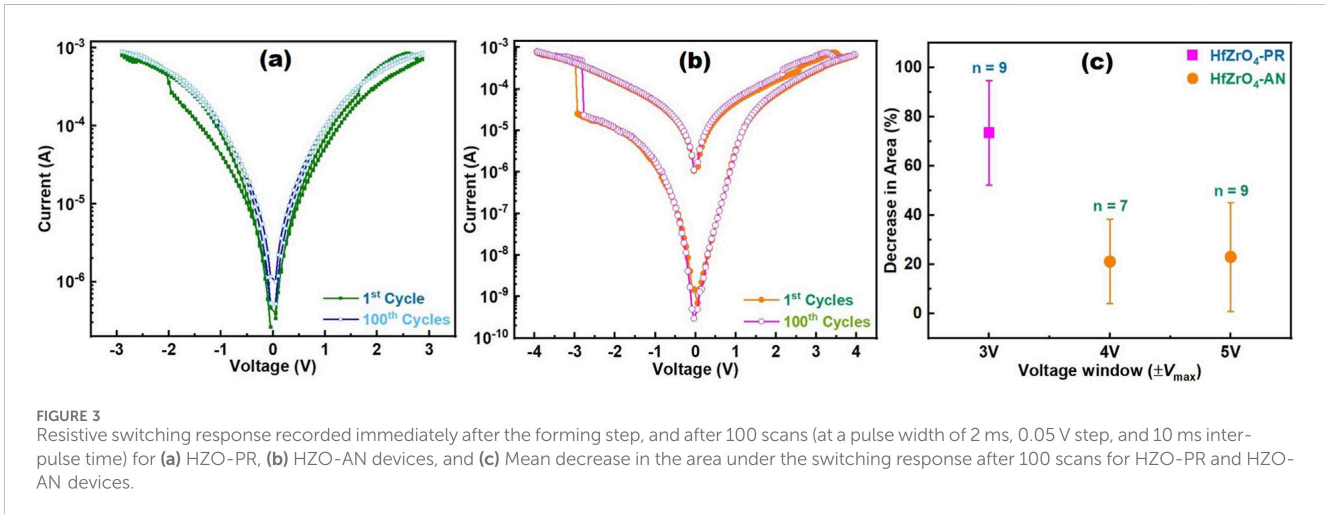

FIGURE 3
Resistive switching response recorded immediately after the forming step, and after 100 scans (at a pulse width of 2 ms, 0.05 V step, and 10 ms inter-pulse time) for **(a)** HZO-PR, **(b)** HZO-AN devices, and **(c)** Mean decrease in the area under the switching response after 100 scans for HZO-PR and HZO-AN devices.

measurement is performed (Serb et al., 2015), and the outcomes are displayed in Figure 2d. The measurement is carried out using a set switching tolerance of 30%; however, a lower value of 10% is also used, and the results are shown in Supplementary Figure Sb (see supporting information). The resistive switching happens at around 2.25 V (between 2 and 2.5 V) in the case of HZO-PR devices; however, a larger voltage pulse of approximately 3.75 (around 3.5–4 V) is required to show an appreciable difference in the resistance states (i.e., HRS and LRS states) of the HZO-AN device.

Additionally, switching cycling was done at the pulse width of 2 ms in the voltage of ±3 V and ±4 V for HZO-PR and HZO-AN devices, respectively, which verifies the device stability in an extreme condition of high voltage ramp and fast steps as shown in Figures 3a,b. The HZO-PR devices are relatively less stable as compared to the HZO-AN devices. There is a systematic decrease in the hysteresis window with potential cycling for HZO-PR, whereas there is no significant difference between the first switching cycles and to 100th switching cycles as observed in HZO-AN. This signifies a certain modification at the HZO/TiN interface after annealing at 400 °C for 60 s. Similar cycling performance was carried out for multiple devices to investigate the consistency in the applied potential across several devices. The decrease in the hysteresis (as determined from the decrease in the area under the switching cycle) for 9 (7 devices for 4 V) devices is shown in Figure 3c. The HZO-PR shows a mean relative decrease in the area of 73.5% after 100 scans at a voltage of 3 V. On the other hand, HZO-AN shows much better retention of the hysteresis corresponding to a marginal drop in area (21%–23%) after 100 scans at 4 and 5 V. These outcomes confirm the superior stability of HZO-AN devices over the HZO-PR devices.

3.3 Effect of SET/RESET on the stability and switching characteristics of HZO devices

To understand the switching behaviour of HZO-PR and HZO-AN devices, the switching voltages of the device at various stages of testing (i.e., switching cycling at various voltages) are estimated from the switching responses. The analysis is performed by controlling the potential cycling (10 *I-V* scans) at different maximum voltage amplitudes. The measurement is also carried out using a dedicated, newly formed device. Initially, the device was subjected to the forming process to create a switchable device as described earlier. The switching responses were measured at the various voltages until the ability of the device to switch is lost. Supplementary Figures S5,S6 (see supporting information) show the selected switching response for HZO-PR and HZO-AN, respectively.

The mean switching voltages (V_{sw}) for HZO-PR and HZO-AN are shown in Figure 4a. There is a systematic increase in the V_{sw} for both positive and negative polarity with an increase in the maximum voltage amplitude. Further, consistent switching in HZO-PR is observed at a maximum voltage amplitude window of 2.5–4.0 V, while at the higher voltages, the device loses its switching capability. Similarly, for HZO-AN, stable switching is observed in the voltage range of 4.0–5.5 V, with maximum hysteresis observed at 5.0 V. The V_{sw} for 5 different devices is shown in Figure 4b, and consistency in the values is established. The standard deviation in the V_{sw} for HZO-PR is relatively small, while the values are larger in the case of HZO-AN. This can be due to the thermal treatment of the HZO layer, which may induce randomness in the ions/vacancies movement while switching, which further leads to the non-linear resistive switching, bipolar switching, and multilevel switching characteristics (Jiang et al., 2021; Napari et al., 2024; Funck and Menzel, 2021; Giovinazzo et al., 2019; Quinteros et al., 2021; Loy et al., 2020; Rahaman et al., 2017; Banerjee et al., 2017; Yadav et al., 2025; Kumar et al., 2025). Figure 4c shows the selected *I-V* scans for an HZO-AN device, and as observed in the figure, the V_{sw} in the negative potential changes with cycles. Similarly, the fifth I-V scan from 5 different devices also behaves quite differently in terms of Vsw, even though they have similar hysteresis characteristics as shown in Figure 4d. This is very common in Hf-based memristive devices as reported earlier (Jiang et al., 2021; Napari et al., 2024; Funck and Menzel, 2021; Giovinazzo et al., 2019; Quinteros et al., 2021; Loy et al., 2020; Rahaman et al., 2017; Banerjee et al., 2017; Yadav et al., 2025; Kumar et al., 2025; Saleh et al., 2014).

Figure 4e shows the retention (600 s) at different voltages (±2.5 and ±4 V) for the HZO-PR device; the corresponding switching responses are shown in Supplementary Figure S7a (see

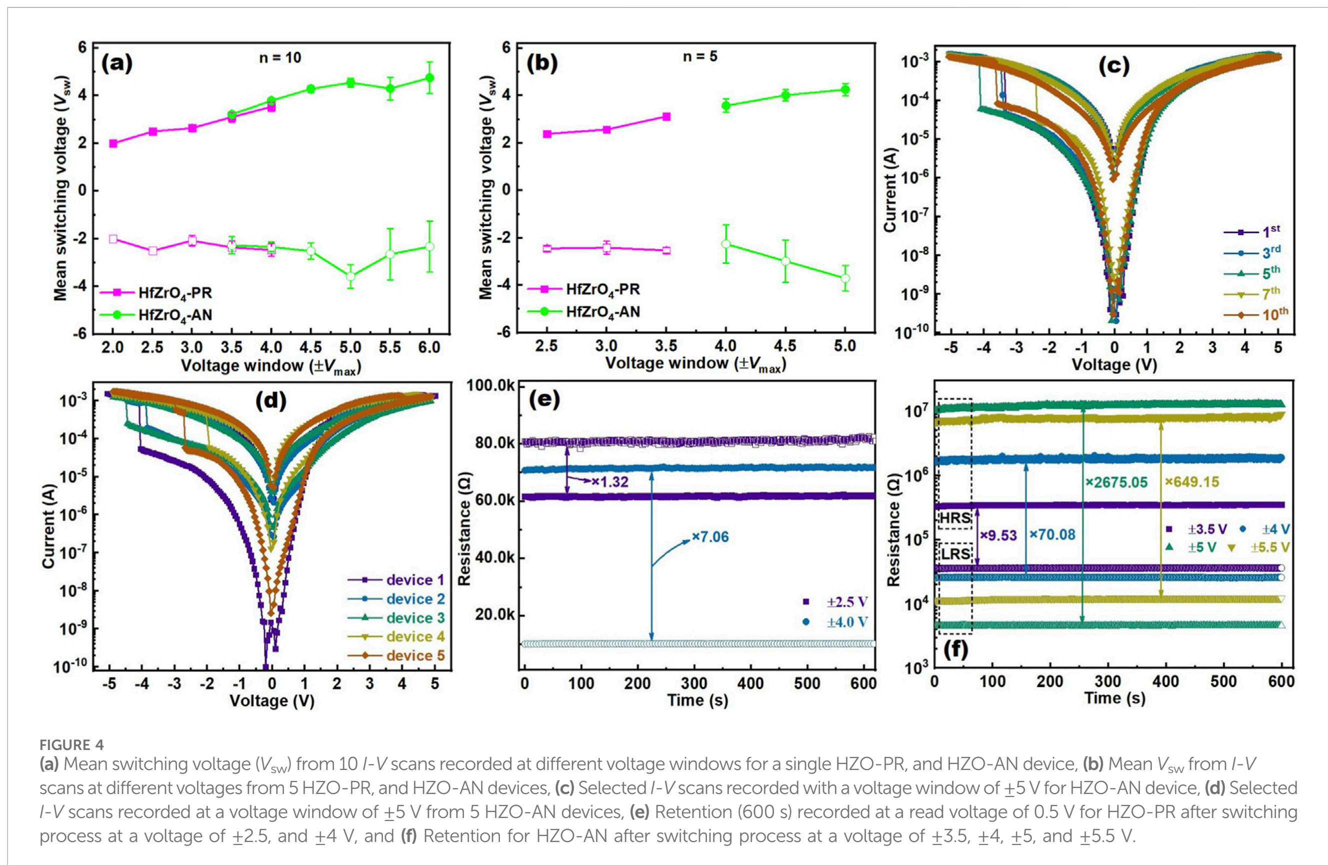

FIGURE 4
(a) Mean switching voltage (V_{sw}) from 10 *I-V* scans recorded at different voltage windows for a single HZO-PR, and HZO-AN device, **(b)** Mean V_{sw} from *I-V* scans at different voltages from 5 HZO-PR, and HZO-AN devices, **(c)** Selected *I-V* scans recorded with a voltage window of ±5 V for HZO-AN device, **(d)** Selected *I-V* scans recorded at a voltage window of ±5 V from 5 HZO-AN devices, **(e)** Retention (600 s) recorded at a read voltage of 0.5 V for HZO-PR after switching process at a voltage of ±2.5, and ±4 V, and **(f)** Retention for HZO-AN after switching process at a voltage of ±3.5, ±4, ±5, and ±5.5 V.

supporting information). Retention measurements are performed in a controlled way. First, a SET/RESET voltage sweep is applied. After that, the retention test is conducted without doing any additional I-V cycling (full positive-to-negative sweep) between the measurements at different voltages. The HRS/LRS ratio increases with the increasing maximum voltage, from ~1.3 times to ~7 times. Moreover, stable retention features (a stable resistance with time) are evident at both voltages. However, there is a subtle difference in the SET/RESET polarity for ±2.5 and ±4 V. In the case of ±2.5 V, the device is switched to SET condition by applying a positive voltage sweep, and a stable resistance of ~62 kΩ (LRS) is observed in the read step, whereas, by applying a negative voltage sweep, the device is RESET (or HRS), exhibiting a read resistance of ~81.5 kΩ. Additionally, when the voltage is raised to ±4 V, the device behaves exactly opposite to what was observed at ±2.5 V. In this case, the device is RESET (or HRS) (~72 kΩ) with a positive voltage sweep, and is SET (or LRS) (~10.2 kΩ) with a negative voltage sweep. In the case of HZO-AN devices, the controlled SET/RESET *I-V* (see Supplementary Figure S7b in supporting information), followed by retention measurements (see Figure 4f) recorded at ±3.5, ±4, ±5, and ±5.5 V, indicate the stable SET-RESET polarity. Herein, it should be noted that under all the potential ranges, the device RESET (or HRS) is with a positive voltage sweep, and SET (or LRS) under a negative voltage sweep. Additionally, the HRS/LRS ratio shows an incremental trend with the voltage till ±5 V (HRS/LRS of 2675.05) and then drops to a lower value of 649.15 at ±5.5 V, which can be due to the softness in the oxide layer under a higher electric field.

The HRS/LRS ratios are remarkably high for the above HZO-AN device. In most experiments, the maximum HRS/LRS ratio observed is around 100 to 200 times and is typically observed at a SET/RESET voltage of 5 ± 0.5 V. The notably high ON/OFF ratio in our fabricated devices may be due to the controlled experimental sequence as adopted during device fabrication, post-annealing process, and optimized electrical measurements. Generally, the devices are cycled at various maximum potentials before recording the final retention, whereas for the controlled experiments, the *I-V* cycling step is completely avoided. Moreover, the HRS and LRS values are varied with the potential; as mentioned earlier, it is expected that the HRS is potential dependent; however, the slight variation in the LRS is unexpected. Therefore, as observed, for the $Hf_1Zr_1O_4$ composite material, both HRS and LRS states are input potential dependent.

3.4 Pulse programmability

Lastly, the programmability of the devices is investigated by applying voltage pulses at various voltages, followed by a read voltage of 0.5 V for 10 min. Initially, the device is formed following the pulse forming process as explained earlier, and then the device is turned to LRS by subjecting it to a voltage pulse with a multiplicative pulse width progression to a fixed resistance of 10 kΩ. This way, the multilevel memory states and their stability can be assessed. The HZO-AN device is SET (or LRS) by applying a negative voltage amplitude, while a

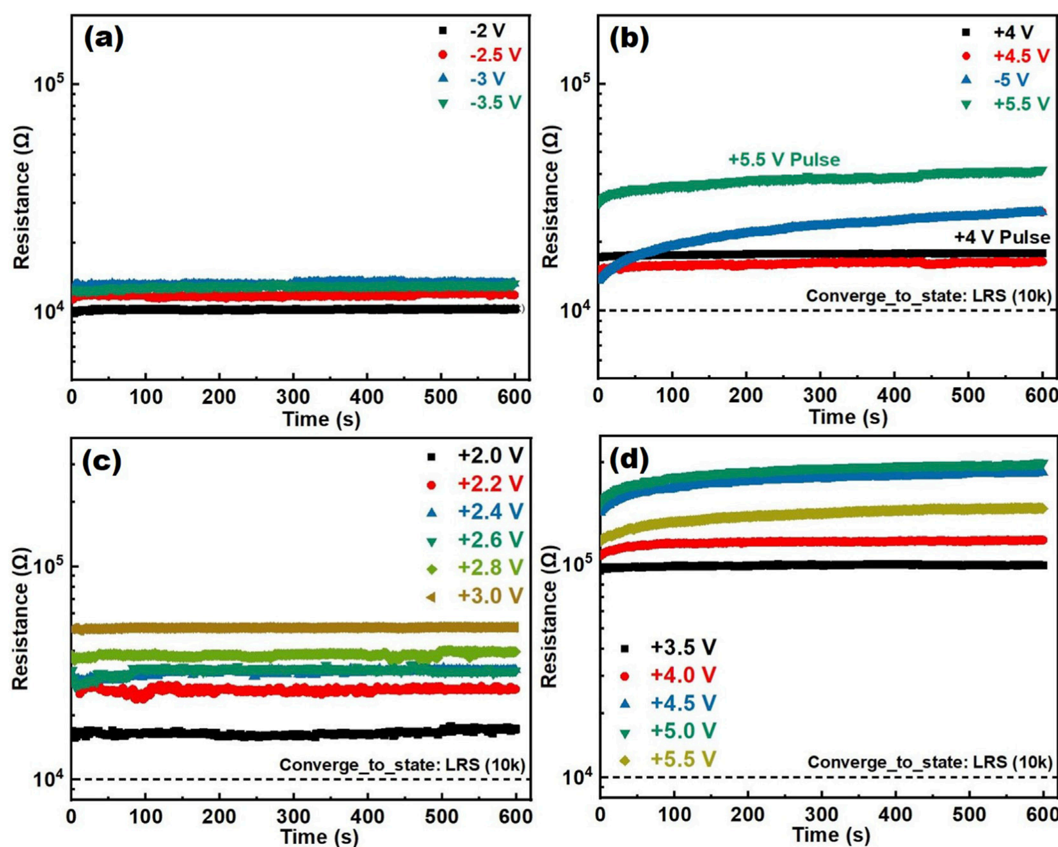

FIGURE 5
Retention curve at different HRS formed after the voltage pulse step at various voltages **(a,b)** $HfZrO_4$-PR, and **(c,d)** $HfZrO_4$-AN. The LRS is achieved by multiplicative pulse width voltage progression to a fixed resistance of 10 kΩ.

positive voltage pulse is used for RESET (or HRS). Once the retention at HRS is completed, then the device is again SET (or LRS) by multiplicative voltage pulse width progression to 10 kΩ using a negative polarity pulse. The measurement is then repeated at various RESET voltages to form multilevel HRS. The change in the SET/RESET polarity in the case of HZO-PR is already discussed in the earlier section.

Supplementary Figure S8 (see supporting information) shows the multiplicative pulse width progression to a fixed resistance of 10 kΩ after each voltage pulse measurement for HZO-PR and HZO-PR devices. For HZO-PR, the device is SET (or LRS) by a positive polarity multiplicative pulse width progression, while, for most of the RESET (or HRS) voltage pulse, negative polarity is required. However, after performing the pulse at −3.5 and −5 V, the device switching polarity changes, and a positive pulse voltage of 4 and 5.5 V is used to RESET (or HRS). Subsequently, the LRS is made by subjecting a negative polarity multiplicative pulse width progression. The retention at various HRS states for HZO-PR is shown in Figures 5a,b.

Moreover, as shown in Supplementary Figure S8 (see supporting information), the HRS polarity is interchanged for the HZO-PR devices under the high voltage sweep, while the HRS polarity is consistent for all voltage sweeps in HZO-AN devices, as shown in Figures 5c,d. The consistency in the HRS (or RESET process) in HZO-AN devices can be associated with the modification in the device interface due to the annealing process. On the other hand, device interface stability is not good in the HZO-PR devices, which further affects the voltage polarity under different scan ranges. The results show stable retention of HRS for different HRS. Apart from the sudden change in the SET/RESET polarity, the device performance is satisfactory. The retention plot after various HRS for HZO-AN is shown in Figures 5c,d; the corresponding multiplicative pulse width progression to LRS is shown in Supplementary Figure S8b (see supporting information). It is observed that the device shows stable retention at various HRS, and the SET/RESET polarity is consistent for all measurements performed at various voltage amplitude pulses. Moreover, HRS to LRS (~10 kΩ) increases systematically, and beyond 3.5 V, there is a noticeable increment in the hysteresis loop (HRS to LRS values). Supplementary Table S1 (see supporting information) shows the comparison between this work and other state-of-the-art works reported in the literature (Wang et al., 2019; Zhao and Yan, 2020; Yu et al., 2021; Liu et al., 2024).

4 Conclusion

In summary, the thermal ALD-grown HfZrO4-based ferroelectric memristive is reported in which the switching layer

was deposited at 250 °C by a super-cycle approach, maintaining a 1: 1 ratio of HfO_2 and ZrO_2. Both HZO-PR and HZO-AN require an initial electroforming process, and the values of forming voltage were ~5.3 and ~9.2 V, respectively. Moreover, the XRD analysis indicates the formation of nano-crystallinity/multiple phases in the switching layer after the annealing process. On the other hand, the XPS outcomes revealed an increase in the sub-oxide (HfO_{2-x}/ZrO_{2-x}) content in the annealed film. Additionally, the HZO-AN also exhibits a significant increment in the hysteresis ON/OFF ratio as compared to HZO-PR, but was observed at a relatively higher voltage amplitude (≥3.5 V). The HZO-PR is not very stable during switching operation, and a ~73% drop in area under the hysteresis curve was observed after the 100th switching cycle, while only a ~22% drop was observed in the HZO-AN, signifying its superior stability. Additionally, the switching voltages for both HZO-PR and HZO-AN devices are dependent on the applied voltage amplitude; however, in the case of HZO-PR, SET/RESET polarity also influences the LRS/HRS. The HZO-AN devices exhibit a bipolar switching response in which a positive RESET and a negative SET are applied. Furthermore, the devices also show stable retention at various HRS, and the SET/RESET polarity is consistent for all the voltages. However, the HZO-PR devices exhibit a change in voltage polarity with increasing applied voltage amplitude, but show a stable retention property. Therefore, the obtained outcomes strongly suggest that the fabricated devices can efficiently demonstrate the in-memory computation, multilevel data computation, and can also be useful as synaptic devices in analog and neuromorphic computing.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary Material, further inquiries can be directed to the corresponding authors.

Author contributions

RR: Conceptualization, Data curation, Formal Analysis, Investigation, Methodology, Validation, Visualization, Writing – original draft, Writing – review and editing. SS: Conceptualization, Formal Analysis, Investigation, Methodology, Validation, Visualization, Writing – review and editing. SK: Data curation, Formal Analysis, Investigation, Validation, Visualization, Writing – original draft, Writing – review and editing. HL: Data curation, Formal Analysis, Validation, Visualization, Writing – review and editing. DY: Data curation, Formal Analysis, Validation, Visualization, Writing – review and editing. AT: Data curation, Formal Analysis, Methodology, Validation, Visualization, Writing – review and editing. TP: Conceptualization, Data curation, Formal Analysis, Funding acquisition, Project administration, Resources, Supervision, Visualization, Writing – review and editing.

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Conflict of interest

The author(s) declared that this work was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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Supplementary material

The Supplementary Material for this article can be found online at: https://www.frontiersin.org/articles/10.3389/fnano.2026.1729291/full#supplementary-material

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