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EDITED BY

Tongbo Wei,
Chinese Academy of Sciences (CAS), China

REVIEWED BY

Yuyao Kuang,
University of California, Irvine, United States
Li Xuyang,
Xi'an Technological University, China

*CORRESPONDENCE

Jidong Jin,
✉ jinjidong@hanyang.ac.kr
Jiawei Zhang,
✉ Jiawei.Zhang@email.sdu.edu.cn

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Enhanced electrical stability of IGZO thin-film transistors using atomic layer deposited Al₂O₃/HfO₂ dual-layer gate insulator

Shaocong Lv¹, Weilin Wang¹, Shuaiying Zheng¹,
Chengyuan Wang¹, Qian Xin¹, Yuxiang Li¹, Aimin Song^{2,3},
Jaekyun Kim⁴, Jidong Jin^{4*} and Jiawei Zhang^{1*}

¹Shandong Technology Center of Nanodevices and Integration, School of Integrated Circuit, Shandong University, Jinan, China, ²Institute of Nanoscience and Applications, Southern University of Science and Technology, Shenzhen, China, ³Department of Electrical and Electronic Engineering, University of Manchester, Manchester, United Kingdom, ⁴Department of Photonics and Nanoelectronics, Hanyang University, Ansan, Republic of Korea

This study investigates the stability of positive bias temperature stress (PBTS) in bottom-gate indium-gallium-zinc-oxide (IGZO) thin-film transistors (TFTs) incorporating atomic layer deposited Al₂O₃/HfO₂ dual-layer gate insulators (GIs). By optimizing the thicknesses of the Al₂O₃ and HfO₂, hydrogen diffusion from the GI into the IGZO layer is effectively controlled and electron traps at the IGZO/GI interface are mitigated. The optimal dual-layer GI configuration for IGZO TFTs is identified as 15 nm Al₂O₃ on 5 nm HfO₂, resulting in an exceptionally low threshold voltage shift of -0.02 V under PBTS at 125 °C for 10⁴ s. Additionally, the device exhibits excellent electrical performance, with a saturation mobility of 11.61 cm²/Vs, a subthreshold swing of 114 mV/dec, and a threshold voltage of -0.23 V. These results highlight the potential of IGZO TFTs with dual-layer GIs for advanced integrated circuit applications.

KEYWORDS

IGZO, thin-film transistor, PBTS, high-k, dual-layer gate insulator

1 Introduction

Indium-gallium-zinc-oxide (IGZO) thin-film transistors (TFTs) have attracted significant attention for various display applications due to their high carrier mobility, large-area uniformity and low-temperature processability (Ide et al., 2019; Shim et al., 2020; Shi et al., 2021; Geng et al., 2023; Çeliker et al., 2024; Bao et al., 2025). Furthermore, IGZO TFTs have demonstrated compatibility with back-end-of-line (BEOL) processes, making them suitable for integration into complex integrated circuits (Chi et al., 2016; Yu et al., 2016; Duan et al., 2022; Izukashi et al., 2025).

High-k dielectric materials, such as Al₂O₃ (Ma et al., 2018a), HfO₂ (Ma et al., 2018b), Ta₂O₅ (Chiu et al., 2010) and ZrO₂ (Lee et al., 2010) have been employed as gate insulators (GIs) to enable low-voltage operation in IGZO TFTs while maintaining good device performance. The choice of high-k dielectrics significantly impacts the electrical

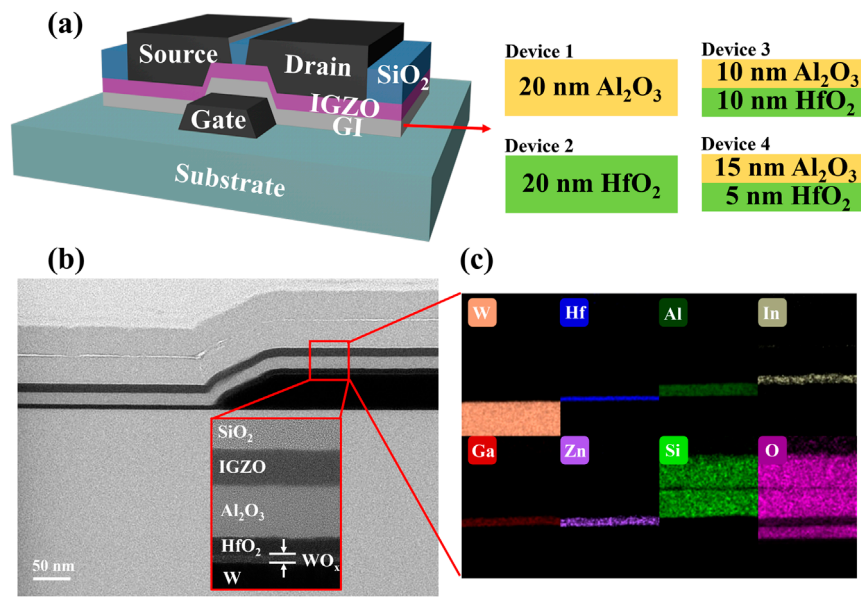
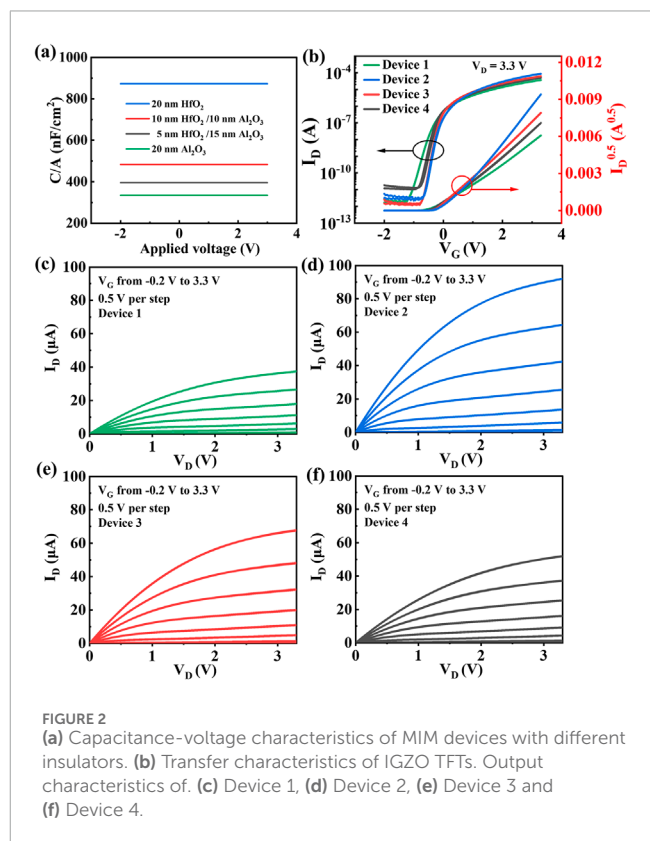


FIGURE 1 (a) Schematic of IGZO TFTs with different dielectric layers. (b) Cross-sectional TEM image and (c) EDS image of Device 4.

performance of IGZO TFTs, particularly in terms of leakage currents, interface quality and driving current capability (Lee et al., 2013; Geng et al., 2014; Li et al., 2022). In addition to the impact of high-k dielectrics on electrical characteristics, device reliability under bias stress must be rigorously evaluated. For BEOL compatible IGZO TFTs in integrated circuit applications, positive bias temperature stress (PBTs) is a critical metric for assessing device reliability (Kim et al., 2023; Kim et al., 2024). Therefore, ensuring high PBTs stability is essential for the development of robust and efficient integrated circuit technologies.

Both electron trapping at the IGZO/GI interface and hydrogen (H) diffusion from the GI into the IGZO channel strongly influence device reliability of IGZO TFTs under PBTs (Kim et al., 2023; Kim et al., 2024; Liu et al., 2024b). Notably, the H content in the GI critically affects PBTs stability (Kim et al., 2024; Lin et al., 2024; Liu et al., 2024a; Liu et al., 2024b; Lv et al., 2025). Under PBTs, it should be noted that high H content in the GI can diffuse into the IGZO channel and form donor-like states (Kim et al., 2024; Liu et al., 2024b). These states increase free electron density and passivate IGZO/GI interface defects, leading to negative threshold voltage shifts (ΔV_{TH}) (Kim et al., 2024; Liu et al., 2024b; Lv et al., 2025). In contrast, low H content in the GI may leave IGZO/GI interface traps unpassivated under PBTs, resulting in positive ΔV_{TH} (Kim et al., 2024; Lv et al., 2025). Therefore, precise control of H concentration in the GI is essential for achieving reliable PBTs stability with minimal ΔV_{TH} .

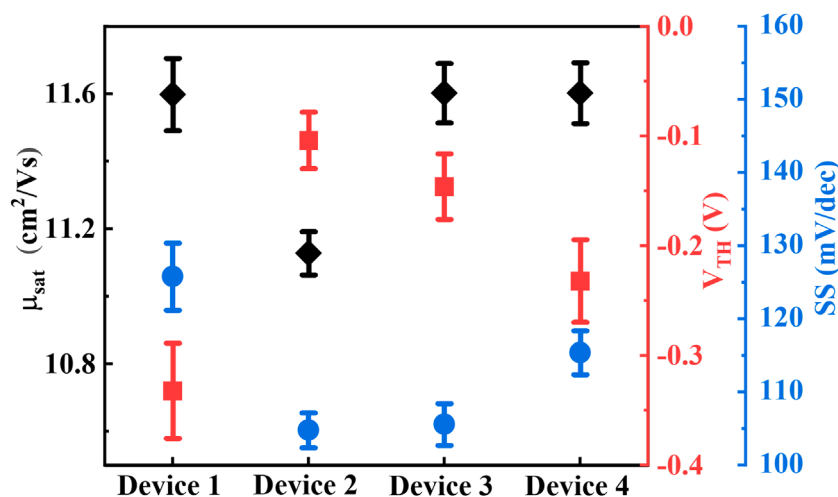
In this study, we introduce a H-regulated GI strategy for IGZO TFTs, enabled by an engineered Al₂O₃/HfO₂ dual-layer stack that precisely modulates H diffusion and electron trapping dynamics. The H content in the GI was controlled by adjusting the thickness of HfO₂ and Al₂O₃ during the atomic layer deposition (ALD) process. Through combined PBTs measurements, X-ray photoelectron spectroscopy (XPS) and time-of-flight secondary ion mass spectrometry (TOF-SIMS) analyses, we identified H



concentration and transport pathways within the GI as the primary factors governing the direction and magnitude of ΔV_{TH} for IGZO TFTs under PBTs. It was found that the device based on a 15 nm Al₂O₃/5 nm HfO₂ dual-layer GI effectively passivate electron traps at the IGZO/GI interface without inducing significant H diffusion under PBTs. As a result, the device demonstrates

TABLE 1 Electrical characteristics of IGZO TFTs with different GIs.

IGZO TFT	Al ₂ O ₃ /HfO ₂ (nm)	V _{TH} (V)	SS (mV/dec)	μ _{sat} (cm ² /Vs)	D _{it} (cm ⁻² /eV)
Device 1	20/0	-0.33	128	11.64	2.31 × 10 ¹²
Device 2	0/20	-0.10	105	11.14	4.22 × 10 ¹²
Device 3	10/10	-0.16	106	11.66	2.21 × 10 ¹²
Device 4	15/5	-0.23	114	11.61	2.23 × 10 ¹²

FIGURE 3 Statistical data of μ_{sat}, V_{TH}, and SS of IGZO TFTs.

excellent PBTS stability with a ΔV_{TH} of -0.02 V at 125 °C for 10^4 s. Furthermore, the device demonstrated excellent electrical performance. These characteristics demonstrate that this approach offers a promising pathway toward IGZO TFTs with both high stability and excellent electrical performance for display and integrated circuit technologies.

2 Experimental section

Figure 1a illustrates the schematic diagram of bottom-gate IGZO TFTs with different GIs: 20 nm Al₂O₃ (Device 1), 20 nm HfO₂ (Device 2), 10 nm Al₂O₃/10 nm HfO₂ (Device 3), and 15 nm Al₂O₃/5 nm HfO₂ (Device 4). Initially, a 50-nm-thick W gate electrode was deposited on the SiO₂/Si substrate by radio-frequency (RF) sputtering at room temperature in an Ar atmosphere. Then, ALD was employed to deposit the GI materials at 200 °C. Trimethylaluminum (TMA) and tetrakis(dimethylamido)hafnium (TDMAH) served as the precursors for Al₂O₃ and HfO₂ respectively, with H₂O used as the oxidant. Following the GI deposition, a 12 nm IGZO active channel layer was deposited by RF sputtering using an IGZO target with an In:Ga:Zn ratio of 2:2:1 at room temperature in Ar. Subsequently, the GI and IGZO channel layers were annealed at 400 °C for 1 h in O₂. A 100 nm SiO₂ passivation layer was then deposited by plasma-enhanced chemical vapor deposition (PECVD), and the source/drain regions were defined by reactive

ion etching. The source and drain electrodes, consisting of 10 nm indium tin oxide and 100 nm tungsten, were deposited by RF sputtering. Finally, the IGZO TFTs underwent a post-deposition annealing at 400 °C for 1 h in O₂. The channel width and length of the TFTs were 35 μm and 5 μm, respectively.

Electrical characteristics were measured using a Keysight B2902A semiconductor parameter analyzer. PBTS tests were conducted in a chamber probe station with a hot chuck at both 25 °C and 125 °C. XPS spectra were recorded using a ThermoFisher ESCALAB 250Xi system. The spatial distribution of H was determined by TOF-SIMS depth profiling using an ION TOF-SIMS 5 instrument. The cross-sectional transmission electron microscopy (TEM) image and energy dispersive spectroscopy (EDS) elemental line scans were obtained using a high-resolution TEM (HRTEM, Talos F200X, Thermo Fisher Scientific).

3 Results and discussion

Figure 1b shows the cross-sectional TEM image of Device 4, revealing uniform, well-defined interfaces between all layers. Figure 1c shows EDS mapping of W, Hf, Al, In, Ga, Zn, Si, and O for Device 4, confirming uniform growth and distribution of all elements.

Figure 2a shows the capacitance densities of various dielectric materials measured using a metal-insulator-metal (MIM) device

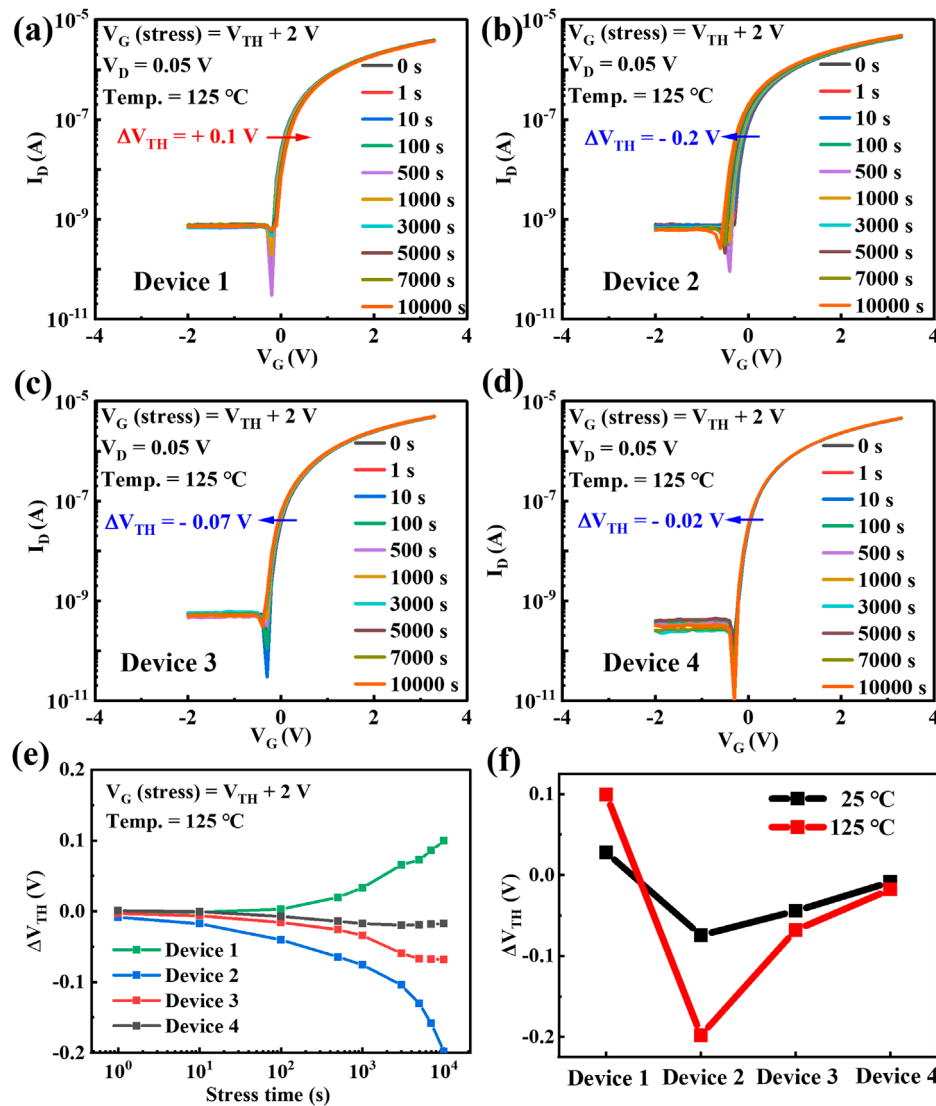


FIGURE 4 Variations in transfer curves with the evolution of stress time for (a) Device 1, (b) Device 2, (c) Device 3 and (d) Device 4 under PBTs (125 °C). Summary of (e) stress-time-dependent variations in ΔV_{TH} and (f) ΔV_{TH} at 10^4 s under 25 °C and 125 °C.

structure. The capacitance densities for 20 nm Al_2O_3 , 20 nm HfO_2 , 10 nm $\text{Al}_2\text{O}_3/10$ nm HfO_2 , and 15 nm $\text{Al}_2\text{O}_3/5$ nm HfO_2 are 334.16, 873.18, 483.34, and 395.14 nF/cm^2 , respectively. Figure 2b presents the transfer curves of the IGZO TFTs with different GIs, while Figures 2c–f show the corresponding output curves. Key device parameters, including threshold voltage (V_{TH}), subthreshold swing (SS), field-effect saturation mobility (μ_{sat}), and interface trap density (D_{it}), were extracted from the transfer curves and are summarized in Table 1. The μ_{sat} and SS were calculated using the following Equations 1, 2 (Lee and Chung, 2023):

$$\mu_{\text{sat}} = \frac{2L}{WC_{\text{ox}}} \left(\frac{d\sqrt{I_D}}{dV_G} \right)^2 \quad (1)$$

$$SS = \left(\frac{d \log(I_D)}{dV_G} \Big|_{I_{\text{max}}} \right)^{-1} \quad (2)$$

where L is the channel length, W is the channel width, C_{ox} is the gate capacitance per unit area, I_D and V_G are the drain current and gate voltage, respectively. The V_{TH} was defined at a drain current of $(W/L) \times 10$ nA. The D_{it} can be estimated using the following Equation 3 (Jin et al., 2023):

$$D_{\text{it}} = \left(\frac{SS \log(e)}{kT/q} - 1 \right) \frac{C_{\text{ox}}}{q^2} \quad (3)$$

where k is the Boltzmann constant, T is temperature, and q is the elementary charge. When comparing single-GI devices, Device 2 (20 nm HfO_2) shows a more positive V_{TH} (-0.10 V) and higher D_{it} ($4.22 \times 10^{12} \text{ cm}^{-2}/\text{eV}$) than Device 1 (20 nm Al_2O_3), while its μ_{sat} is slightly reduced due to the higher D_{it} . Devices 3 and 4, which employ $\text{Al}_2\text{O}_3/\text{HfO}_2$ bilayer GIs, exhibit intermediate V_{TH} and SS values, while maintaining high μ_{sat} ($\sim 11.6 \text{ cm}^2/\text{Vs}$) and relatively low D_{it} ($\sim 2.2 \times 10^{12} \text{ cm}^{-2}/\text{eV}$), demonstrating that bilayer GIs can

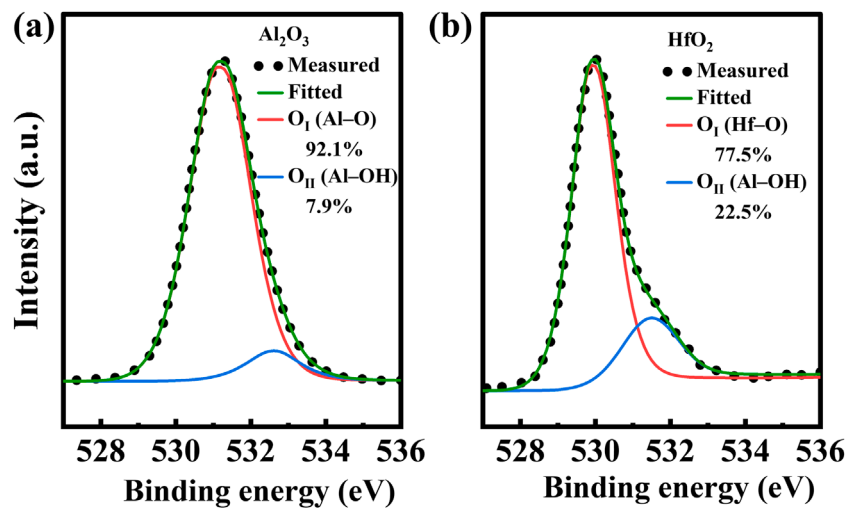


FIGURE 5
The XPS spectra of (a) Al₂O₃ film and (b) HfO₂ film with a thickness of 20 nm.

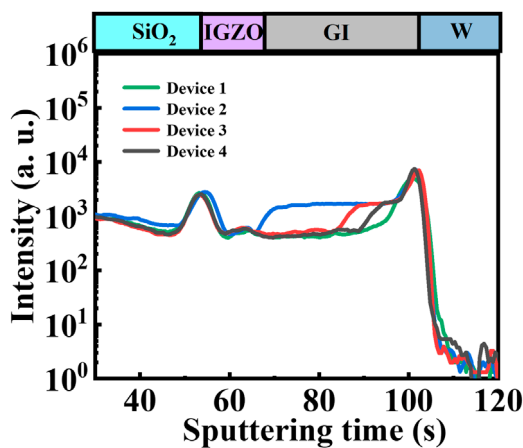


FIGURE 6
TOF-SIMS depth profiles of the intensities of H across the samples with different GIs.

effectively balance V_{TH} control, SS, and interface quality. To assess reproducibility, 5 additional devices of each type were tested, and the results are summarized in Figure 3, showing consistent device performance across samples.

In addition to electrical performance, the reliability of these devices under PBTS was further evaluated, revealing distinct behaviors depending on the GI configuration, with Device 4 exhibiting the highest PBTS stability. The PBTS test results are shown in Figures 4a–d. During the PBTS measurements, a gate-stress voltage, V_G (stress) = $V_{TH} + 2$ V, was applied for 10^4 s under vacuum conditions at both 25 °C and 125 °C. The transfer curves were measured at $V_D = 0.05$ V. The devices exhibit distinct behaviors under PBTS conditions, depending on the type of GI. Device 1 shows a positive ΔV_{TH} of +0.1 V at 125 °C, indicating that electron trapping at the IGZO/Al₂O₃ interface or within the Al₂O₃ layer

is the dominant degradation mechanism (Kim et al., 2023). In contrast, Device 2 exhibits a negative ΔV_{TH} of –0.2 V under identical conditions due to excessive free carrier generation in IGZO, likely caused by H diffusion from the HfO₂ GI (Lee et al., 2023). In Devices 3 and 4, which utilize a dual-layer GI, lower ΔV_{TH} values were observed under PBTS at 125 °C for 10^4 s. Device 3 exhibits a ΔV_{TH} of –0.07 V, while Device 4 exhibits a ΔV_{TH} of –0.02 V. These enhanced PBTS stabilities suggest that the implementation of a dual-layer GI can effectively mitigate electron trapping at the IGZO/GI interface through H diffusion. For effective H diffusion, the H content must differ significantly between the two layers of the dual-layer GI. The variations in ΔV_{TH} for IGZO TFTs with different GIs under PBTS at 125 °C are presented in Figure 4e. Clearly, Device 4 shows the best PBTS stability. Figure 4f illustrates the ΔV_{TH} values measured at both 25 °C and 125 °C for IGZO TFTs with different GIs subjected to PBTS for 10^4 s, with Device 4 exhibiting the smallest variation in ΔV_{TH} .

The chemical bonding states at the surfaces of HfO₂ and Al₂O₃ gate dielectrics were examined using XPS. Figure 5 illustrates the O 1s core-level XPS spectra for both the HfO₂ and Al₂O₃ films, where O_I represents the metal–O bond, while O_{II} represents the metal–OH bond. The area ratios of –OH in the HfO₂ and Al₂O₃ films are 22.5% and 7.9%, respectively, indicating a significantly higher H content in the HfO₂ film. Figure 6 presents TOF-SIMS analysis of the devices, revealing that the H intensity in HfO₂ reaches 1.69×10^3 a.u., approximately four times higher than in Al₂O₃. For the devices with a dual-layer Al₂O₃/HfO₂ GI, a pronounced H gradient is clearly observed across the interface.

Figure 7 presents the schematic energy band diagrams of IGZO TFTs incorporating different GI configurations under PBTS, constructed from the combined PBTS, XPS and TOF-SIMS analyses. The distinct PBTS behaviors observed across the devices can be directly attributed to differences in the H content of the Al₂O₃ and HfO₂ layers. Figure 7a represents Device 1 (single Al₂O₃ GI) and indicates that the markedly low H concentration in the Al₂O₃ GI suppresses H-related reactions (Lv et al., 2025). As a result, electron

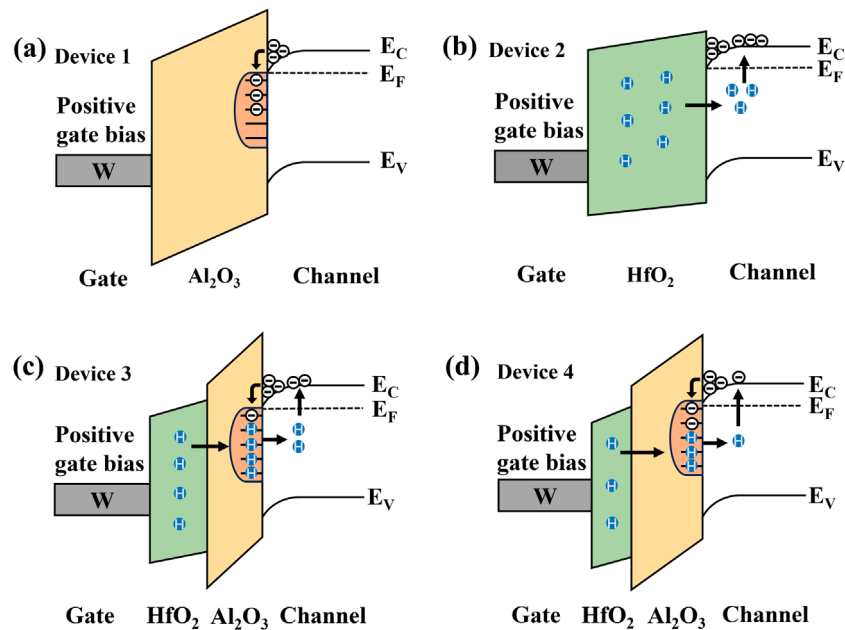


FIGURE 7 Energy band diagrams of (a) Device 1, (b) Device 2 (c) Device 3 and (d) Device 4 under PBTS.

trapping at the IGZO/GI interface or within the GI becomes the dominant PBTS mechanism, yielding a positive ΔV_{TH} under PBTS (Kim et al., 2024; Lv et al., 2025). In Figure 7b, representing Device 2 (single HfO₂ GI), the significantly higher H concentration in the HfO₂ GI promotes H diffusion from HfO₂ into the IGZO channel. This migrated H acts as a shallow donor and increases the free electron density (Lee et al., 2023), leading to donor-generation-dominated and a negative ΔV_{TH} . Figures 7c,d correspond to Devices 3 and 4, which employ dual-layer Al₂O₃/HfO₂ GIs. These stacked GIs provide enhanced PBTS stability by simultaneously moderating H diffusion and reducing interface-related electron trapping. Notably, Device 4, with its thinner HfO₂ layer, further restricts H diffusion into the IGZO channel. Such controlled H diffusion is unique to Device 4 and results in the most balanced and stable PBTS behavior among all devices examined.

4 Conclusion

In this work, we demonstrate a H-regulated GI design based on a Al₂O₃/HfO₂ stack that enables fine control over H diffusion and electron trapping in IGZO TFTs. XPS and TOF-SIMS analyses collectively reveal that H concentration and transport pathways within the GI critically determine the sign and magnitude of ΔV_{TH} for IGZO TFTs under PBTS. The optimized IGZO TFT with 15 nm Al₂O₃/5 nm HfO₂ GI demonstrates an exceptionally low ΔV_{TH} of -0.02 V under PBTS at 125 °C for 10⁴ s. Moreover, the optimized TFT exhibits excellent electrical performance, featuring a μ_{sat} of 11.61 cm²/Vs, a SS of 114 mV/dec, and a V_{TH} of -0.23 V. These findings offer significant potential for integrated circuit applications, where excellent electrical performance and high stability are essential.

Data availability statement

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation.

Author contributions

SL: Methodology, Software, Writing – review and editing, Conceptualization, Writing – original draft, Formal Analysis, Data curation. WW: Methodology, Writing – original draft, Formal Analysis, Data curation. SZ: Software, Conceptualization, Methodology, Writing – review and editing. CW: Writing – review and editing. QX: Writing – review and editing. YL: Writing – review and editing. AS: Writing – review and editing. JK: Writing – review and editing. JJ: Methodology, Writing – original draft, Data curation, Investigation, Writing – review and editing. JZ: Conceptualization, Methodology, Supervision, Funding acquisition, Investigation, Writing – review and editing, Formal Analysis, Project administration, Writing – original draft, Data curation, Resources, Validation.

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Conflict of interest

The author(s) declared that this work was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Generative AI statement

The author(s) declared that generative AI was not used in the creation of this manuscript.

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