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EDITED BY
Leszek A. Majewski,
The University of Manchester,
United Kingdom

REVIEWED BY
Yousfi Abderrahim,
Universite Mohamed El Bachir El Ibrahimi de Bordj Bou Arreridj, Algeria
Adam Szyszka,
Wrocław University of Technology, Poland

*CORRESPONDENCE
Lakshmi Priya K.,
lk4899@srmist.edu.in

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Influence of polarization engineering in $In_xAl_yGaN_{1-x-y}$ back-barrier on AlGaN coupled channel MOS-HEMT with HfO_2 gate dielectric for millimeter wave application

Lakshmi Priya K* and Karthik S

Department of Electronics and Communication Engineering, Faculty of Engineering and Technology, SRM Institute of Science and Technology, Vadapalani Campus, Chennai, Tamilnadu, India

This study investigates a high-performance double-tiered T-gate AlGaN coupled-channel MOS-HEMT that incorporates an InAlGaN back-barrier and employs HfO_2 as the gate dielectric. The device performance is analysed using Sentaurus TCAD simulations, which include mobility models, hydrodynamic and thermodynamic effects, piezoelectric polarization, and impact ionization models. The epitaxial structure utilizes an AlGaN coupled-channel to enhance carrier confinement and a lattice-matched InAlGaN back-barrier to minimize buffer leakage. As a result, the device achieves a drain current of 1.19 A/mm, a peak transconductance of 400 mS/mm, a drain-induced barrier lowering (DIBL) of 72 mV/V, and a threshold voltage (Vth) shift of −2 V. The double-tiered T-gate with field-plate extensions significantly improves breakdown performance, achieving a blocking voltage of 640 V. Furthermore, experimental measurements demonstrate a cut-off frequency (fT) of 206 GHz with a gate length of 60 nm. The device exhibits a substantial improvement in current drive due to the use of a graded AlGaN coupled-channel combined with an InAlGaN back-barrier, compared to conventional AlGaN composite-channel HEMTs. Additionally, the proposed design demonstrates enhanced frequency performance, making it a promising solution for high-efficiency power switching and millimetre-wave applications.

KEYWORDS

AlGaN/GaN, MOSHEMT, InAlGaN back barrier, coupled channel, HfO2 dielectric

1 Introduction

The field of wide-bandgap semiconductor technology has seen significant growth, with AlGaN/GaN high-electron-mobility transistors (HEMTs) becoming an important choice for radio frequency (RF) and power electronic applications (Chow and Tyagi, 1994; Teo et al., 2021). Compared to traditional silicon-based transistors, these devices offer several advantages, such as higher electron mobility, better breakdown voltage, and stable performance at high operating temperatures (Fletcher and Nirmal, 2017). The shift toward III-nitride semiconductor materials has accelerated due to the increasing performance demands of 5G communication systems, satellite technologies, and next-generation radar

systems, where silicon-based devices face limitations (Piotrowicz et al., 2018). III-nitride materials naturally exhibit polarization effects that create a two-dimensional electron gas (2DEG), which plays a key role in improving device performance. Over the past few decades, advances in material growth and fabrication techniques have led to noticeable improvements in the DC and RF performance of AlGaN/GaN HEMTs (Del Alamo, 2011).

Recent research has focused on using alloyed back-barrier layers to improve electron confinement in the channel, leading to better device efficiency. Ternary alloys such as AlGaN and InGaN have been widely studied, but each material presents challenges. InGaN has a narrower bandgap, which allows for higher electron density but can also introduce alloy disorder and reduce performance reliability. On the other hand, AlGaN back-barriers provide better electron confinement but may cause parasitic conduction and make high-quality epitaxial growth more difficult (Murugapandiyan et al., 2019; Kalita et al., 2023; Kim et al., 2019).

To overcome these issues, researchers have proposed using quaternary alloys such as InAlGaN. By carefully adjusting the indium and aluminium compositions, these materials can achieve lattice matching with GaN, which reduces defect density and minimizes piezoelectric effects. Additionally, InAlGaN allows better control over the bandgap and polarization properties, resulting in improved electrostatic control, better carrier confinement, and reduced buffer leakage (Wang et al., 2019; Noual et al., 2023). Its good thermal properties and lattice compatibility also make it easier to integrate into device structures and support scalability. When combined with graded channel engineering techniques, these materials enable the design of transistors with better linearity and efficiency (Upadhyay and Chattopadhyay, 2019).

Initially, AlGaN/GaN MOS-HEMTs used SiO_2 as the gate dielectric. However, researchers have shifted toward using high-k dielectric materials such as ZnO, Al_2O_3, and HfO_2 due to their better electrical performance (Yue et al., 2008). Among these, HfO_2 is particularly effective because of its high dielectric constant and wide bandgap, which help improve the saturation drain current, reduce gate leakage, and allow better threshold voltage control. These features are essential for achieving enhancement mode operation and maintaining linearity in RF and high-power applications (Abderrahim et al., 2018; Dube et al., 2024).

The use of a graded coupled channel further improves electron confinement by keeping carriers closer to the conducting channel, which enhances overall efficiency (Sandeep and Pravin, 2021). In addition, T-gate structures with field-plate extensions have been shown to improve breakdown voltage by distributing the electric field more evenly and reducing localized field peaks near the gate edge (Fletcher et al., 2022). With continuous progress in material design, device architecture, and fabrication techniques, GaN-based HEMTs now achieve high current-driving capability, stable threshold voltage, low on-resistance, and excellent linearity at RF frequencies. These developments make them strong candidates for future high-frequency and high-power system-on-chip (SoC) applications.

In this study, the Sentaurus TCAD simulation platform is used to analyze and enhance the DC and RF performance of MOS-HEMTs by employing lattice-matched InAlGaN back-barriers, positioned between the buffer and substrate, with HfO_2 used as the gate dielectric. The impact of incorporating an AlGaN coupled channel on overall device performance is also investigated. Section 2 describes the proposed device structure and simulation methodology, Section 3 presents the simulation results along with a comparative analysis against existing literature, and Section 4 summarizes the key findings and their significance for the development of next-generation transistors.

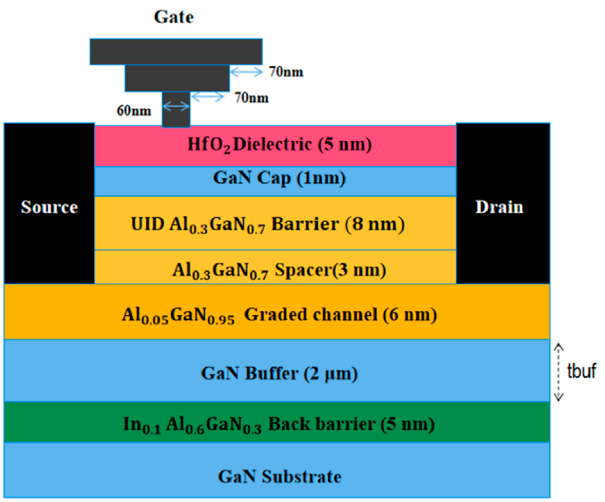

FIGURE 1
Schematic cross-sectional view of the proposed AlGaN coupled-channel MOS-HEMT featuring an InAlGaN back-barrier and an HfO_2 gate dielectric.

2 Device architecture and formulation of the analytical framework

The proposed high-electron-mobility transistor (HEMT) structure, illustrated in Figure 1, was designed and simulated using the Sentaurus TCAD platform to optimize both DC and RF performance. The device is built on a GaN substrate, which provides mechanical stability and efficient thermal dissipation. Above this, a 2-µm undoped GaN buffer layer reduces lattice strain and supports the heterostructure layers. A 5-nm $In_{0·1}Al_{0·6}GaN$ back-barrier is incorporated beneath the buffer to improve vertical electron confinement, reduce buffer leakage, and enhance 2DEG density. On top of the buffer, a 6-nm graded $Al_{0·05}Ga_{0·95}N$ subchannel layer is implemented to enhance electron confinement, improve carrier mobility, and reduce polarization-induced depletion. The barrier region consists of a 3-nm $Al_{0·3}Ga_{0·7}N$ spacer and an 8-nm unintentionally doped $Al_{0·3}Ga_{0·7}N$ barrier layer, which work together to form a strong polarization field, facilitating high 2DEG density at the heterointerface. A 1-nm GaN cap layer protects the underlying barrier and maintains a smooth surface for reliable Schottky gate formation. To further enhance device performance, a 5-nm HfO_2 high-k gate dielectric is employed, which improves electrostatic gate control, minimizes gate leakage, and enables better threshold voltage tuning.

The design prevents carrier spillover and improves 2DEG density and thermal performance. The gate structure uses a dual-tiered T-gate with a gate length of 60 nm and lateral extensions

TABLE 1 Main parameters of proposed MOS-HEMT.

Parameter	Value	Unit
Gate length (Lg)	60	nm
Field Plate length of T gate (LFP)	70	nm
Total gate length (Lg)	150	nm
Gate-to-source gap (Lsg)	100	nm
Gate-to-drain gap (Lgd)	300	nm
Drain electrode length (Ld)	500	nm
Dielectric (HfO_2) thickness	10	nm
GaN cap layer thickness	1	nm
AlGaN barrier thickness	10	nm
AlGaN channel thickness	3	nm
AlGaN Graded channel thickness	6	nm
GaN buffer thickness	2	μm
AlInGaN back-barrier thickness	5	nm
GaN substrate thickness	2	μm

of 70 nm on each side. The gate-to-source and gate-to-drain distances are 0.1 μm and 0.3 μm, respectively. A short gate length and optimized gate area reduce parasitic capacitance and improve performance. The gate-to-drain distance (LGD) is larger than the gate-to-source distance (LSG) to maintain a lower electric field near the drain. This layout manages the electric field distribution by concentrating it near the gate and keeping it low at the source and drain, thereby reducing buffer leakage. It also improves breakdown voltage and high-frequency response (Russo and Di Carlo, 2007). The main structural parameters of the proposed MOS-HEMT are listed in Table 1.

For device modelling, drift-diffusion and hydrodynamic transport models are used to analyses carrier mobility and velocity saturation. Thermal models handle self-heating effects, Shockley–Read–Hall recombination accounts for trap-assisted processes, polarization models simulate spontaneous and piezoelectric effects, and impact ionization models evaluate breakdown behavior. Additionally, high-resolution mesh refinement is applied around heterojunctions, gate edges, and contact regions to improve numerical accuracy for electric field and carrier transport simulations, ensuring reliable evaluation of device performance.

The band diagram corresponding to the proposed design is presented in Figure 2. The energy band diagram shows that the InAlGaN back-barrier and graded AlGaN channel enhance electron confinement and 2DEG density, while the high-k HfO_2 gate dielectric improves electrostatic control and reduces leakage, leading to better device performance.

The electrostatic potential distribution within the device is governed by the two-dimensional Poisson's equation, which is

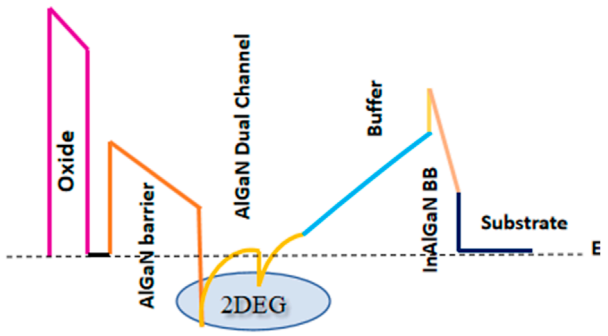

FIGURE 2
Conduction band diagram of the proposed coupled channel MOS-HEMT with the InAlGaN back-barrier.

expressed in Equation 1

$$\frac{\partial^2\phi}{\partial x^2}+\frac{\partial^2\phi}{\partial y^2}=-\frac{qN_D}{\varepsilon_{AlGaN}} \tag{1}$$

where ϕ is the electrostatic potential, N_D is the donor doping concentration, q is the elementary charge, and $\varepsilon_{\mathrm{AlGaN}}$ is the permittivity of the AlGaN barrier. The vertical channel potential profile is approximated by a parabolic function as shown in Equation 2

$$\phi_1(x,y)=\phi_L(x)+C_1(x)(y-t_1) \tag{2}$$

where $\phi_L(x)$ is the potential at the lower interface, $C_1(x)$ is a fitting coefficient, and t_1 is the total thickness from the gate dielectric to the bottom of the graded AlGaN sub-channel, given by Equation 3

$$t_1=t_{\mathrm{cap}}+t_{\mathrm{barrier}}+t_{\mathrm{majorchannel}}+t_{\mathrm{minorchannel}} \tag{3}$$

The 2DEG sheet carrier density at the interface is determined by both electrostatic and polarization effects, is defined in Equation 4

$$n_s=\frac{\varepsilon_{\mathrm{barrier}}}{qt_1}\left[\gamma(\phi_M-\chi_{\mathrm{barrier}})+(1-\gamma)\phi_0-\gamma qN_Dt_1/C_{\mathrm{ox}}+E_F-\Delta E_C\right] \tag{4}$$

where ϕ_M is the metal work function, χ_{barrier} is the electron affinity, ϕ_0 is the surface potential, E_F is the Fermi level, ΔE_C is the conduction band offset, and $C_{\mathrm{ox}}=\varepsilon_{\mathrm{ox}}/t_{\mathrm{ox}}$ is the gate oxide capacitance per unit area. The gate control factor γ accounts for interface traps and is defined in Equation 5

$$\gamma=1/(1+D_{it}q^2/C_{\mathrm{ox}}) \tag{5}$$

with D_{it} representing the interface trap density.

The threshold voltage of the device incorporates the effects of work function difference, oxide and interface trap charges, and polarization charge, is expressed in Equation 6

$$V_T=\phi_{MS}-\frac{t_{\mathrm{ox}}(Q_{\mathrm{ox}}+Q_{\mathrm{it}})}{\varepsilon_{\mathrm{ox}}}-\frac{q\sigma_{\mathrm{tot}}t_1}{\varepsilon_{\mathrm{barrier}}}\left(1+\frac{t_{\mathrm{ox}}qD_{it}}{\varepsilon_{\mathrm{ox}}}\right) \tag{6}$$

where ϕ_{MS} is the metal-semiconductor work function difference, Q_{ox} and Q_{it} are the oxide and interface trap charges, and σ_{tot} is the total polarization charge (Dube et al., 2024).

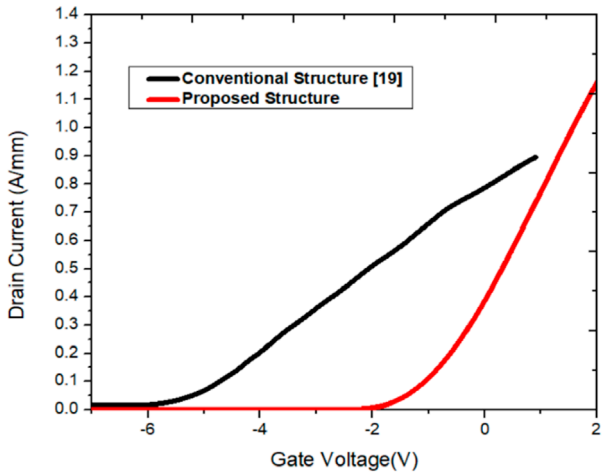

FIGURE 3
Transfer characteristics comparison, showing that the proposed coupled-channel InAlGaN BB MOS-HEMT achieves a higher drain current (1.19 A/mm) than the conventional HEMT, owing to enhanced carrier confinement.

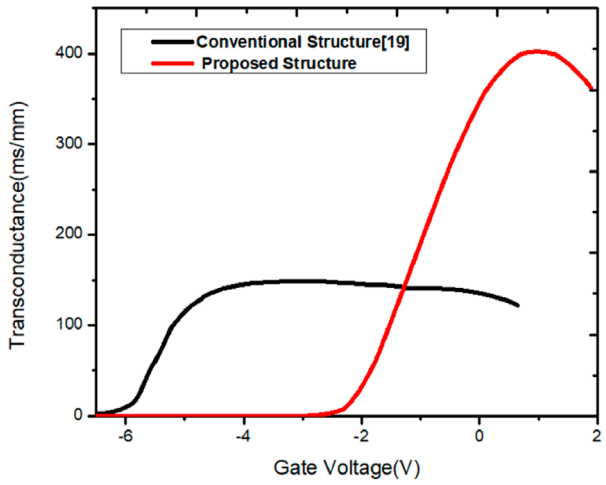

FIGURE 4
Comparison of transconductance (g_m) characteristics between the proposed AlGaN coupled-channel InAlGaN BB MOS-HEMT and the conventional composite-channel HEMT, showing a peak g_m of 400 mS/mm for the proposed device, indicating enhanced channel modulation.

In the linear regime, the drain current is described by Equation 7

$$I_D = \mu(E)C_{eq}\frac{W}{2L_{SD}}\left[(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \quad (7)$$

where $\mu(E)$ is the field-dependent mobility, C_{eq} is the equivalent gate capacitance, W is the gate width, L_{SD} is the source-drain spacing, and V_{GS} and V_{DS} are the gate-source and drain-source voltages, respectively.

The small-signal transconductance, which measures the sensitivity of the drain current to the gate voltage, is defined in Equation 8

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad (8)$$

and the cut-off frequency, which characterizes high-frequency response, is given by Equation 9

$$f_T = \frac{g_m}{2\pi C_{eq}} \quad (9)$$

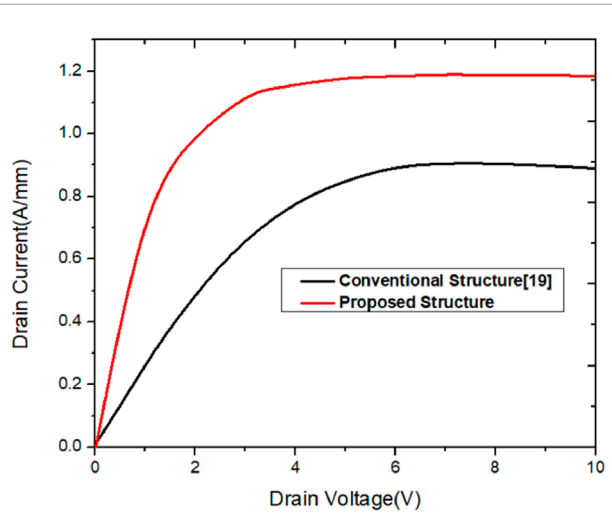

FIGURE 5
Simulated output characteristics of the proposed MOS-HEMT at Vgs = 1 V. The device shows better current saturation and higher output current compared to conventional design.

3 Result and discussion

The performance of the proposed coupled-channel (CC) MOS-HEMT structure, incorporating a high-k HfO_2 dielectric and a lattice-matched InAlGaN back-barrier, has been comprehensively evaluated with a focus on both DC and RF characteristics. The transfer characteristics and transconductance responses are shown in Figures 3, 4, respectively, under a constant drain bias of 6 V. For performance benchmarking, these results are compared with those of the conventional composite-channel HEMT structure. The proposed structure demonstrates significant improvements, achieving a peak drain current of 1.19 A/mm and a maximum transconductance of 400 mS/mm.

Figure 5 presents the simulated output characteristics of the proposed device with the gate biased at 1 V. The results indicate a significant enhancement in drain current drivability and overall output performance compared to the conventional design. This improvement arises from the implementation of a graded $Al_{0.05}Ga_{0.95}N$ coupled channel, which effectively reduces electric field degradation at the source/drain terminals and facilitates efficient carrier transport. The compositional grading introduces a polarization gradient that stabilizes the two-dimensional electron gas (2DEG) density, thereby enhancing current conduction and improving channel control. Furthermore, the incorporation of

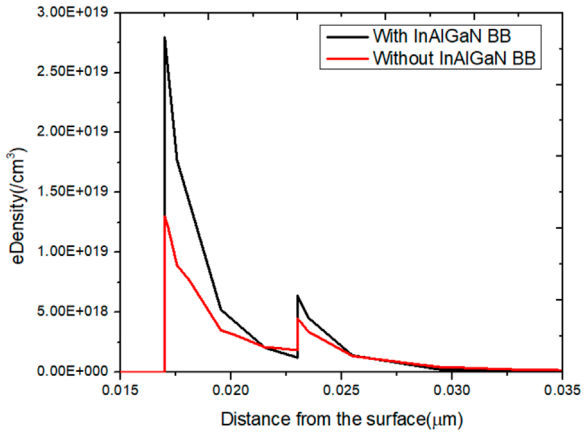

FIGURE 6
Electron concentration diagram of Proposed AlGaN coupled channel MOS-HEMT with and without InAlGaN BB-HEMT.

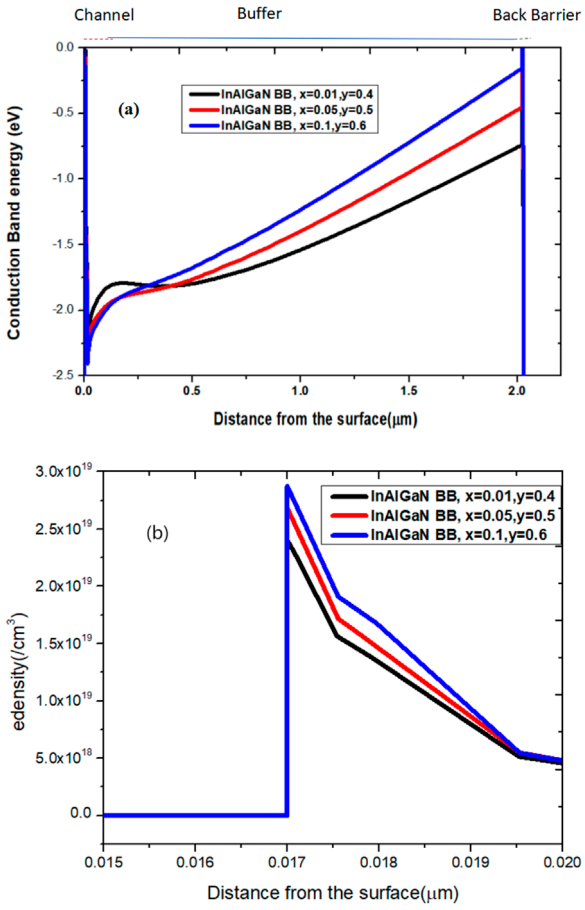

FIGURE 7
(a) Conduction band profile and **(b)** electron concentration distribution in the major channel of the AlGaN coupled-channel MOS-HEMT with an InAlGaN back-barrier (BB), showing the effect of indium (In) and aluminum (Al) mole fraction variation.

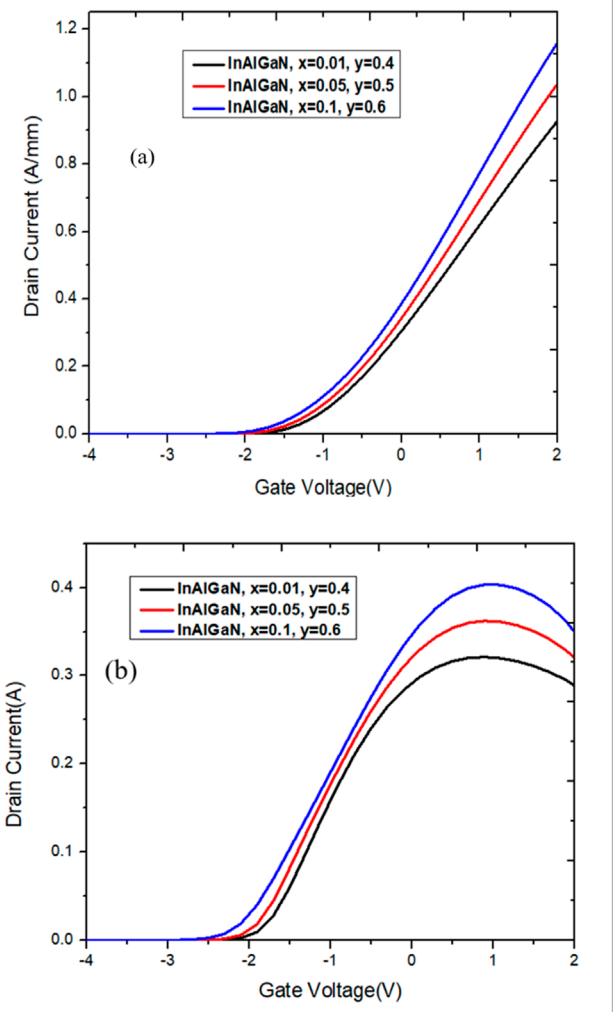

FIGURE 8
(a) Transfer and **(b)** Transconductance profiles for InAlGaN BB-HEMT devices with mole fraction variation, measured at a drain-source voltage of 6 V.

an $In_{0.1}Al_{0.6}Ga_{0.3}N$ back-barrier between the GaN buffer and substrate plays a crucial role in suppressing buffer leakage and strengthening carrier confinement by elevating the conduction band at the GaN/InAlGaN interface.

The incorporation of HfO_2 as the gate dielectric offers several significant advantages for device performance. It enhances charge confinement at the gate-channel interface, minimizes gate leakage, and induces a positive shift in the threshold voltage. Owing to its high dielectric constant, HfO_2 improves gate electrostatics, leading to better control over channel modulation and an enhanced subthreshold slope. Additionally, the introduction of an InAlGaN back-barrier increases the conduction band offset within the channel region, thereby reducing the surface 2DEG density and contributing further to a more positive threshold voltage.

The polarization-induced charge at various heterojunctions is highly dependent on the material composition. As illustrated, increasing the aluminum (Al) content in the AlGaN barrier enhances polarization charge and improves the 2DEG density

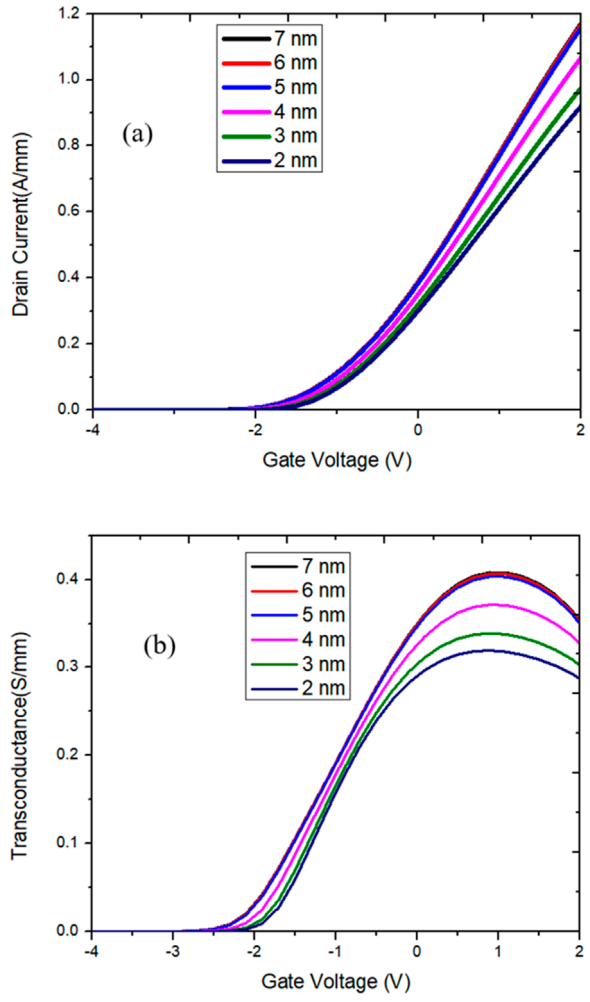

FIGURE 9
(a) Transfer and **(b)** Transconductance profiles for InAlGaN BB-HEMT with different back barrier layer thickness measured at a drain-source voltage of 6 V.

up to an optimal limit. However, exceeding an Al composition of approximately 40% can introduce trap states that negatively impact RF performance, while concentrations below 15% may fail to generate sufficient polarization for robust 2DEG formation. In this study, the Al mole fraction has been carefully optimized within this suitable range to achieve reliable device operation, stronger electron confinement, and improved overall performance.

The simulated 2DEG concentration, shown in Figure 6, reaches approximately 10^{19} cm^{-3} without intentional doping, validating the effectiveness of polarization-induced charge accumulation. The presence of the InAlGaN back-barrier is shown to increase the electron density compared to the structure without it. Positive polarization charge at the AlGaN/GaN interface promotes electron accumulation, while the negative charge at the GaN/InAlGaN interface enhances confinement and suppresses parasitic channel formation. This dual-polarization effect is key to achieving high current drive and minimizing leakage.

Figures 7a,b illustrate the conduction band profile and electron density distribution for three distinct InAlGaN compositions. The spontaneous polarization fields within lattice-matched $In_xAl_yGaN_{1-x-y}$ back-barriers introduce a sharp potential barrier at the GaN buffer interface. The back-barrier effectively elevates the conduction band edge and confines carriers within the channel, minimizing vertical leakage into the substrate.

The corresponding transfer and transconductance characteristics for the three InAlGaN compositions are shown in Figures 8a,b, demonstrating that increasing indium and aluminum content enhances both drain current and transconductance due to stronger channel confinement under different mole fractions.

Figures 9a,b illustrate the impact of back-barrier thickness on device characteristics, with evaluations performed at Lg = 60 nm and Vds = 6 V. As the back-barrier thickness increases, a noticeable negative shift in the threshold voltage is observed, accompanied by an increase in transconductance from 300 mS/mm to 400 mS/mm. This behavior arises from the gradual modulation of the conduction band, which stabilizes the sheet charge distribution. The device exhibits optimal DC performance at a channel thickness below 5 nm, where the maximum drain current increases from 0.94 A/mm to 1.19 A/mm.

Based on the initial simulation results both the maximum drain current and transconductance improve as the InAlGaN back-barrier thickness varies from 2 nm to 5 nm. However, beyond 5 nm, there is no significant enhancement in device characteristics, as shown in the graph. This saturation occurs because, at approximately 5 nm, the conduction band offset and vertical carrier confinement reach their optimum, leading to a well-confined two-dimensional electron gas. Increasing the thickness beyond this point does not further enhance 2DEG density or carrier transport. Moreover, excessively thick back-barrier layers slightly increase parasitic capacitance, which may degrade the device's high-frequency performance.

Figure 10 shows the effect of GaN buffer thickness on the proposed device. As tbuf decreases from 3.0 µm to 2.0 µm, stronger back-barrier coupling enhances 2DEG confinement, resulting in higher Ion, improved transconductance and reduced DIBL. However, further reducing tbuf below 2.0 µm, stronger trap-channel interactions, increases leakage and reduced breakdown voltage. Therefore, 2.0 µm was selected as the optimum thickness, balancing performance improvement and device reliability.

The electric field distribution along the channel is illustrated in Figure 11. In the conventional single-channel configuration, the peak electric field reaches approximately 3 MV/cm near the gate region, which can lead to increased scattering and leakage. In contrast, the proposed graded AlGaN coupled-channel configuration significantly modifies the electric field profile by enhancing the field between the source and gate, thereby enabling smoother band bending. Furthermore, the integration of a field plate with the double-channel architecture effectively redistributes the electric field, leading to improved 2DEG confinement and a higher 2DEG density. This optimized field management not only minimizes interface scattering and leakage but also enhances carrier transport efficiency, demonstrating the

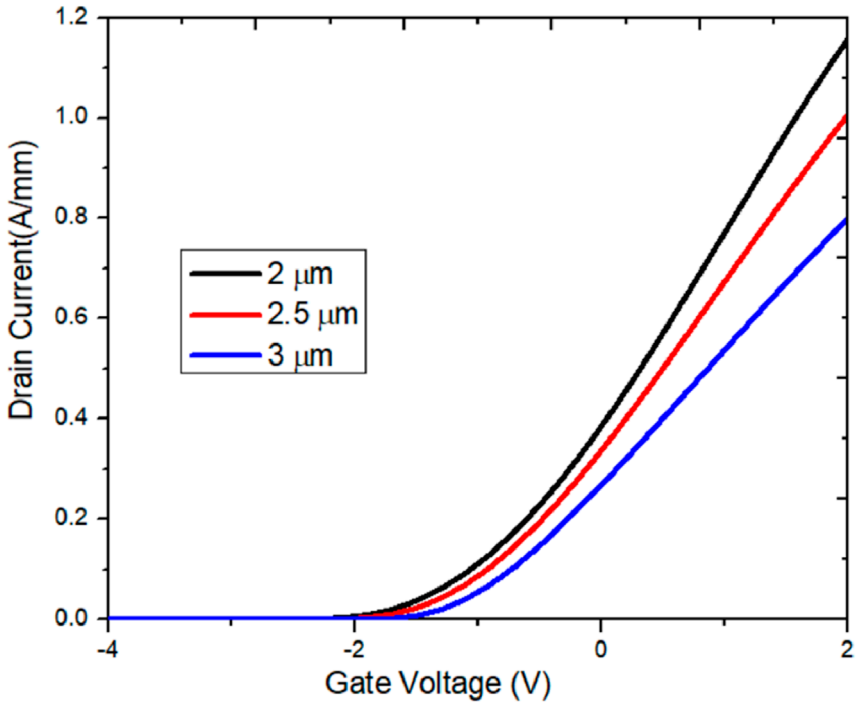

FIGURE 10
Effect of GaN buffer thickness (tbuf) on device performance. Thinner buffers enhance back-barrier control and improve Ion and transconductance but also increase leakage current.

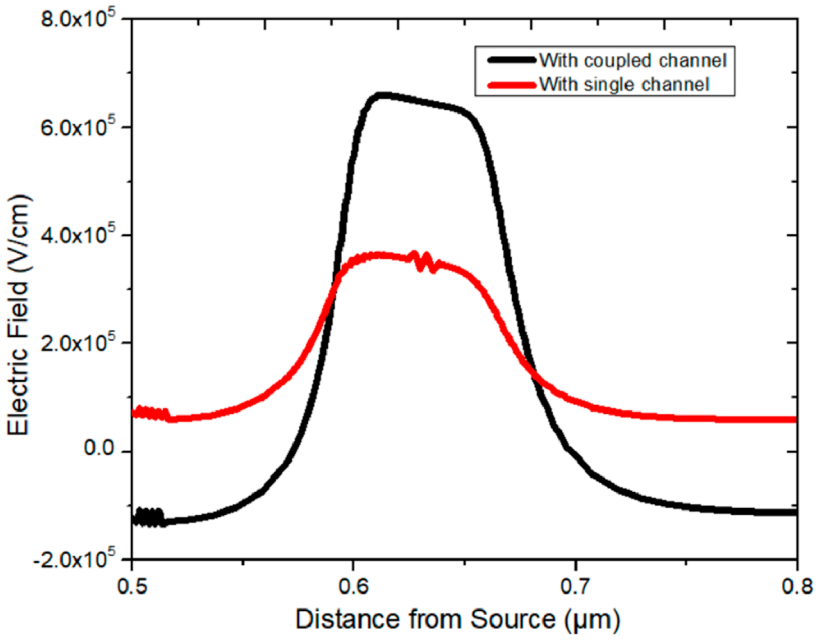

FIGURE 11
Electric field distribution along the source-to-drain direction, comparing cases with and without the coupled-channel.

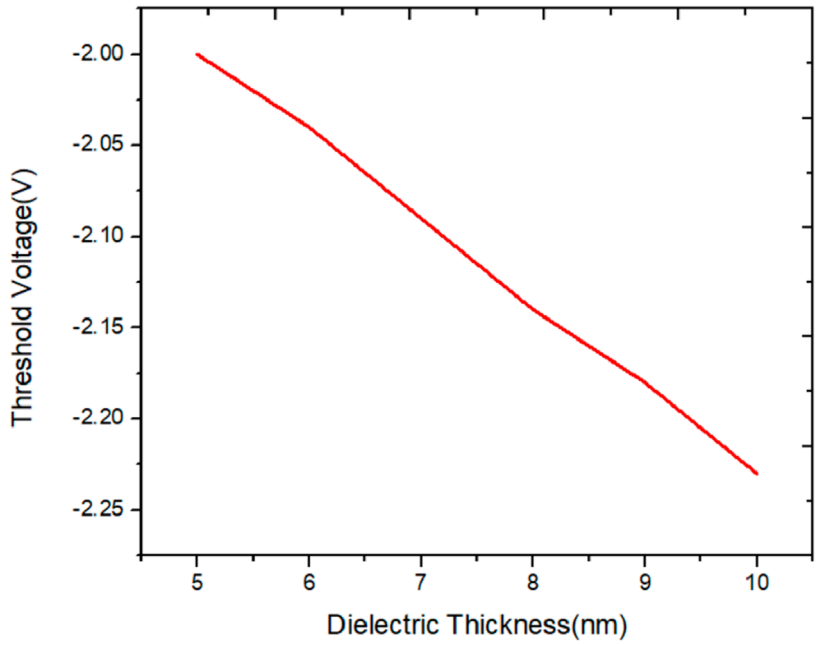

FIGURE 12
Threshold voltage variation as a function of high-k oxide thickness, showing a positive shift with decreasing dielectric thickness.

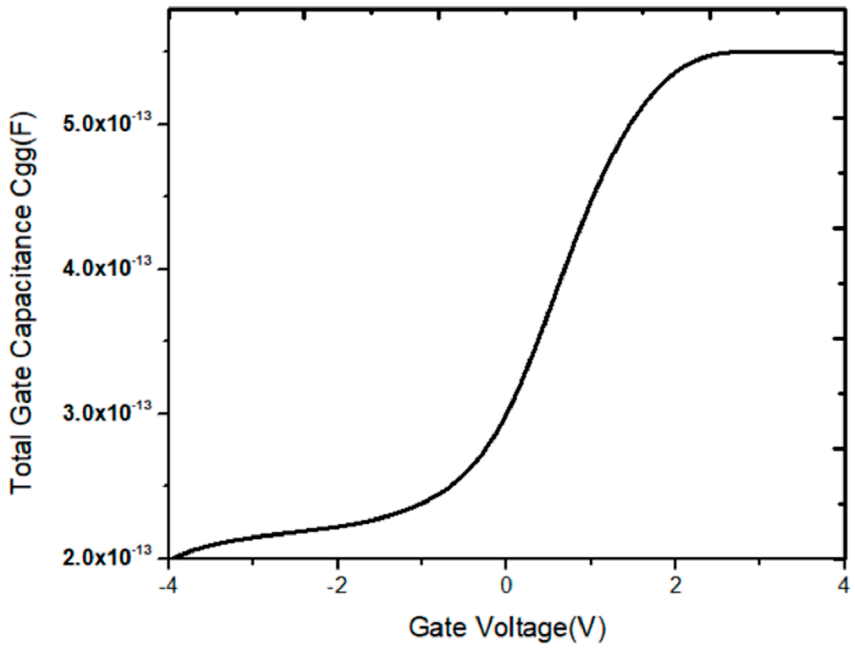

FIGURE 13
Total gate capacitance (Cgg) as a function of gate voltage.

novelty and performance advantage of the proposed device over conventional structures.

Figure 12 illustrates the variation of threshold voltage (Vth) as a function of HfO_2 dielectric thickness. A notable positive shift of up to −2 V is observed when the oxide thickness is scaled down to 5 nm, which can be attributed to improved electrostatic control and suppression of interface trap effects. To evaluate the high-frequency performance of the proposed device, small-signal intrinsic capacitances were extracted. Figure 13 shows the variation of total gate capacitance (Cgg) across a gate voltage sweep from −4 V to +4 V. The proposed HEMT demonstrates a Cgg of approximately 0.5 pF, primarily due to the reduced gate

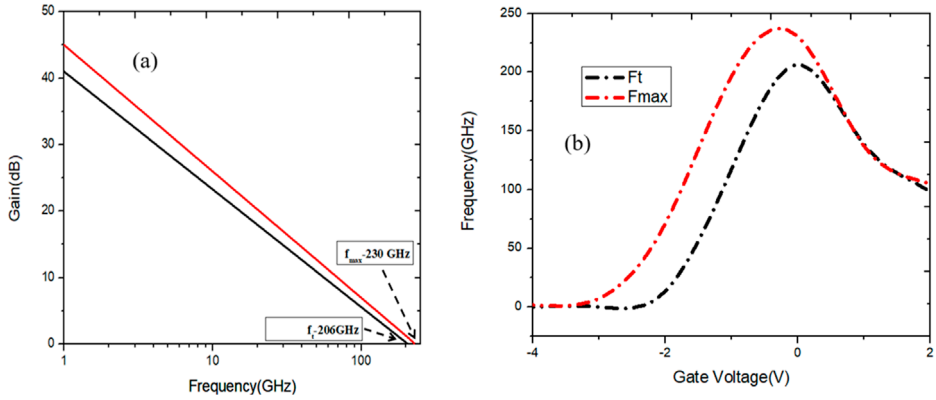

FIGURE 14
(a) Frequency-dependent gain profile of the proposed device. **(b)** Variation of cut-off and maximum frequencies for the MOS-HEMT as the gate voltage is swept from negative to positive, with the drain Voltage held constant at 6 V.

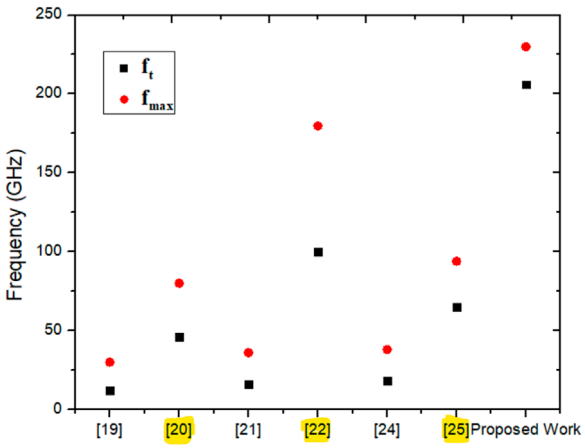

FIGURE 15
Comparison of ft, fmax of several graded back barrier structure from literature.

length and minimized buffer charge. This lower gate capacitance, combined with enhanced transconductance, contributes to improved switching speed and superior overall high-frequency performance.

Figures 14a,b present the gain and frequency characteristics of the proposed device, highlighting its superior high-frequency performance. A significant enhancement in both the cut-off frequency (fT) and the maximum frequency of oscillation (fmax) is observed, demonstrating the device strong potential for RF and high-speed applications. These improvements are primarily attributed to the reduced total gate capacitance (Cgg), efficient channel modulation, and optimized electric field distribution enabled by the proposed structure. Furthermore, Figure 15 compares the frequency characteristics (fT and fmax) of the proposed InAlGaN back-barrier coupled-channel MOS-HEMT with previously reported reference structures, including the composite-channel HEMT (Liu et al., 2005), dual-channel HEMT (Chu et al., 2005), double-channel HEMT with back-barrier (Kamath et al., 2012), AlInGaN/InGaN/GaN DHFET (Adivarahan et al., 2008), and the graded AlGaN back-barrier HEMT (Zhang et al., 2025). The proposed device shows superior performance due to enhanced 2DEG confinement and improved carrier transport. Table 2 provides a comprehensive comparison of the DC performance metrics for various GaN HEMT architectures employing graded back-barriers. The results clearly highlight the proposed design's advantages, including improved drain current, higher transconductance, and superior frequency response, demonstrating its effectiveness for next-generation high-frequency electronic applications.

The implementation of a Tired T-gated structure with a field plate further improves the breakdown voltage, as shown in Figure 16. Simulations were performed with varying field plate lengths (70, 80, and 90 nm), showing that larger plates better redistribute the electric field and suppress gate-drain tunneling.The standard gate structure achieved a breakdown voltage of 604 V, while the T-gated device with a 90 nm field plate exhibited a significantly improved breakdown of 640 V.

4 Conclusion

The comprehensive simulation-based investigation of the proposed AlGaN Coupled-Channel MOS-HEMT, incorporating an InAlGaN back-barrier and high-k HfO_2 dielectric, demonstrates significant performance enhancements tailored for millimeter-wave and high-power electronic applications. The integration of a graded AlGaN coupled channel structure results in enhanced carrier transport and improved current drivability compared to conventional AlGaN CC-HEMT architectures. The engineered InAlGaN back-barrier effectively suppresses parasitic channel formation beneath the 2DEG by enhancing carrier confinement, thereby minimizing leakage and ensuring robust electrostatic control. Key performance metrics include a peak drain current of 1.19 A/mm, a maximum transconductance of 400 mS/mm, and a low specific on-resistance of 0.106 Ωmm, along with a

TABLE 2 Comparison of device performance parameters with previously reported coupled-channel MOS HEMT designs.

References	Peak drain current (mA/mm)	Transconductance (mS/mm)	Threshold Voltage(V)
Zhang et al. (2020)	473	97.9	−9.2
Chu et al. (2005)	800	120	−6
Liu et al. (2005)	900	150	−6
Song et al. (2021)	600	170	−2.5
Sohel et al. (2019)	770	185	−4
Proposed Work	1200	400	−2

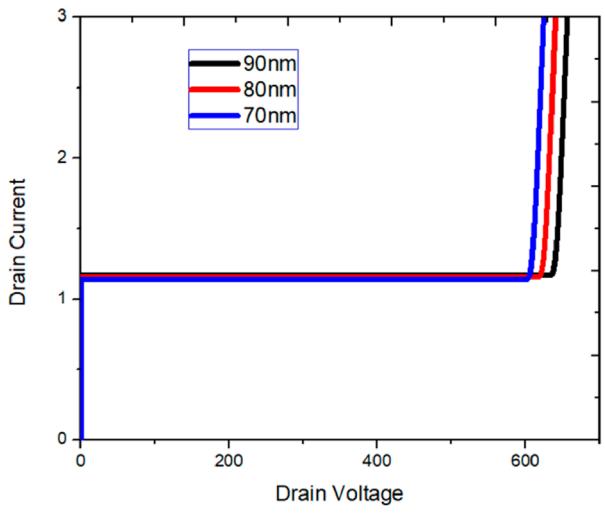

FIGURE 16
The influence of field plate length in a Tired T-gated structure on the breakdown voltage. The device is analyzed with simulations incorporating various field plate deck length (70, 80, and 90 nm).

high breakdown voltage of 640 V achieved via an optimized double-layer T-gate field plate configuration. Furthermore, the incorporation of a 5 nm HfO_2 gate dielectric facilitates a favorable positive shift in threshold voltage (up to −2 V) and contributes to improved gate control. High-frequency characteristics are evidenced by a cut-off frequency (f_t) of 206 GHz at a 60 nm gate length, attributed to the elevated transconductance and reduced total capacitance. Overall, the proposed structure offers a balanced trade-off between high current density and high-frequency response and the breakdown characteristics, establishing it as a strong candidate for next-generation RF power amplifiers and high-performance switching devices.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

Author contributions

LK: Writing – original draft, Writing – review and editing. KS: Writing – original draft, Writing – review and editing.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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