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*CORRESPONDENCE

Frontiers Production Office
✉ production.office@frontiersin.org

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Correction: Processor simulation as a tool for performance engineering

Frontiers Production Office*

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KEYWORDS

high-performance computing (HPC), processor architectures, instruction set extensions, vector instructions, Arm's Scalable Vector Extension (SVE), RISC-V's RVV, performance counters, performance profiles

A Correction on Processor simulation as a tool for performance engineering

by Falquez, C., Long, S., Ho, N., Suarez, E., and Pleiter, D. (2025). *Front. High Perform. Comput.* 3:1669101. doi: 10.3389/fhpcp.2025.1669101

Author Estela Suarez was erroneously assigned to affiliation "SiPEARL, Maisons-Laffitte, France". This affiliation has now been removed for author Estela Suarez.

The conflict of interest statement has been corrected to: The author(s) declared that this work was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

The original version of this article has been updated.