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Correction: Processor simulation as a tool for performance engineering

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high-performance computing (HPC), processor architectures, instruction set extensions, vector instructions, Arm's Scalable Vector Extension (SVE), RISC-V's RVV, performance counters, performance profiles

A Correction on
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Author Estela Suarez was erroneously assigned to affiliation "SiPEARL, Maisons-Laffitte, France". This affiliation has now been removed for author Estela Suarez.

The conflict of interest statement has been corrected to: The author(s) declared that this work was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

The original version of this article has been updated.