A neutral-point voltage balance control method for 3L-NPC converters

Jun Wang*

Department of Electronic Information, Hunan International Economics University, Changsha, Hunan, China

The inherent problem of neutral-point potential imbalance in three-level neutral-point-clamped (3L-NPC) converters increases the risk of overvoltage in switching devices, causes increased output harmonic content, and seriously affects the performance and safe operation of the converters. To achieve neutral-point voltage balance control, this article proposes a neutral-point voltage balance control method based on zero-sequence component injection. The proposed method has the advantage of low computational complexity and can achieve balance control of neutral-point potential under various operation conditions. Finally, the experimental results validated the correctness and effectiveness of the presented method.

KEYWORDS

three-level neutral-point-clamped converter, zero-sequence component injection, neutral-point voltage balance, NPV balance control method, compensated zero-sequence voltage

Introduction

Compared with the traditional two-level inverter, the three-level neutral-point-clamped (3L-NPC) converter has the advantages of large capacity, high output voltage, and low output current harmonic content; therefore, it is widely used in new energy power generation, medium–high voltage, and high-power applications (Lewicki et al., 2024; Lee et al., 2025; Sarker et al., 2024). However, due to its topological structure, there is a problem of neutral-point potential imbalance. The neutral-point potential imbalance not only leads to increased output harmonics but also causes overvoltage damage of power devices, which affects the output performance and safety of the converter (Guo et al., 2022).

With the deepening research on the problem of neutral-point voltage (NPV) balance, some NPV balance strategies have been proposed, mainly divided into hardware balance methods and software balance methods. The former uses additional devices or circuits to balance the neutral-point potential, which requires additional hardware, such as increasing the capacitance of the DC-link capacitors or adding additional voltage equalization circuits. The hardware balance methods increase the system's volume and maintenance costs and also reduce the power density of the system (Von Jouanne et al., 2002; Rivera et al., 2015). The software balancing scheme achieves balance control of the neutral-point potential by improving the control algorithm. Many improved pulse width modulation (PWM) techniques have been developed, which are mainly classified as space vector PWM (SVPWM) and carrier-based PWM (CBPWM) (Chen et al., 2021).

The balance scheme based on SVPWM utilizes the principle that different vectors have different effects on the neutral-point potential to achieve NPV balance

(Liu et al., 2018; Jiang et al., 2020). A vector allocation factor is introduced to adjust the action time of two small vectors. It uses the opposite effect of small vectors on the neutral-point potential to achieve NPV balance (Liu et al., 2018). However, it increases the output harmonic content, and the SVPWM method involves complex trigonometric function calculation and sector judgment. The nearest triangle vectors (NTV) SVM method realizes the NPV balance by selecting proper redundant small vectors (Yamanaka et al., 2002). However, this cannot operate effectively under the conditions of high modulation index and low power factor.

The commonly used methods in CBPWM include dual-modulation signals and zero-sequence voltage injection. The former injects appropriate offset signals into the dual reference signal to generate dual-modulation signals, balancing the DC-link voltages. In Giri et al. (2017) and Giri et al. (2019), dual-modulation signals are generated to balance the capacitor voltage and eliminate its ripple. However, generation of the offset signals relies on real-time acquisition of the voltage vector angles, which involves calculation of inverse trigonometric functions and requires high computational resource overhead. Another approach to achieving NPV balance is to inject a zero-sequence voltage signal into the original modulation signals (Wang et al., 2016; Mukherjee et al., 2019). Zero-sequence voltage affects the direction and magnitude of neutral-point current, thereby achieving NPV balance. Wang et al. (2016) propose a carrier-based PWM strategy with zero-sequence voltage injected for the 3L-NPC inverter, which achieves NPV balancing by decomposing the modulation wave in a specific mode after injecting zero-sequence voltage. This method effectively expands the NPV equilibrium region, but the decomposition of modulated waves involves the calculation of many trigonometric functions, which undoubtedly increases the computational burden. In addition, this method requires prior knowledge of the load power factor, which is difficult to obtain in some practical applications. In Li et al. (2018), a triangle carrier-based discontinuous PWM (TCB-DPWM) method is proposed, which improves system efficiency. However, this method requires calculating the sign of the three-phase voltage and calculating the average neutral-point current within a switching period, which requires multiple multiplication, division, addition, and other operations on the voltage and current. In Zhang et al. (2017) and Mukherjee et al. (2019), the injected zero-sequence voltage signals are generated by a closed-loop controller, which is designed to regulate the deviation of the two DC-link capacitor voltages to be zero. However, the NPV balancing performances, such as steady-state NPV fluctuations and balancing speed, depend on the introduced discontinuity control parameter (Mukherjee et al., 2019).

Some easy-to-implement methods with relatively low computational burden have been proposed (Wan et al., 2021; Alsofyani and Lee, 2021; Wang et al., 2020). The calculation of ideal NP current (Alsofyani and Lee, 2021) and hysteresis capacitance voltage bands (Wang et al., 2020) requires prior knowledge of capacitor parameters, which may affect the performance in cases of unbalanced capacitor parameters or parameter drift caused by aging or heat. The proposed method takes into account the situation of capacitor parameter imbalance.

The neutral-point potential balance is a problem that must be addressed when applying a 3L-NPC converter. Although many scholars have proposed various solutions, most existing solutions

FIGURE 1
Topology of the 3L-NPC converter.
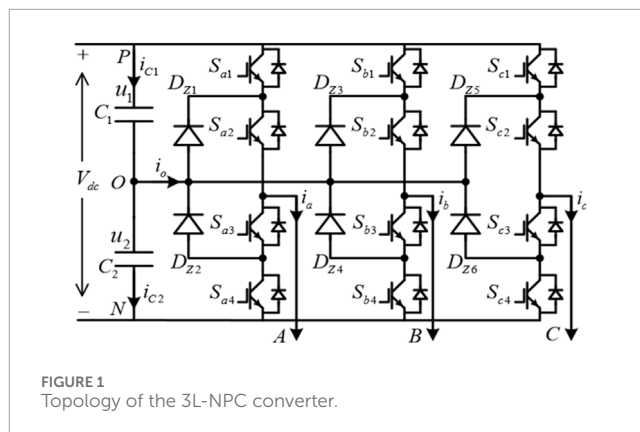
lack low computational complexity characteristics. Therefore, this article proposes a neutral-point voltage balance control method based on zero-sequence component injection for 3L-NPC converters. Compared with most existing CBPWM schemes, the proposed method has the advantage of low computational complexity and good adaptability to operation conditions.

Materials and methods

Figure 1 shows the topology diagram of the 3L-NPC converter. C_1 and C_2 are the upper and lower DC-link capacitors, and u_1 and u_2 are the voltages of the DC-link capacitors. Each phase of the 3L-NPC converter can generate three states, which are defined as "P," "O," and "N."

Based on Kirchhoff's current law, the averaged neutral-point current can be obtained as Equation 1:

$$\overline{i_o} = \overline{i_{C1}} - \overline{i_{C2}} = d_{aO}i_a + d_{bO}i_b + d_{cO}i_c \tag{1}$$

where i_x (x = a,b,c) is the phase current, and d_{xO} {x = a,b,c} is the duty cycle of "O." i_{C1} and i_{C2} are the currents of each capacitor.

It can be seen that the averaged neutral-point current within a switching period is the sum of the instantaneous values of the phase currents in the "O" state of the three-phase system.

NPV balance control method

This section proposes a zero-sequence voltage injection method based on the phase disposition pulse width modulation (PD-PWM) to suppress the neutral-point potential fluctuation of 3L-NPC converters. The averaged neutral-point current can be controlled by injecting zero-sequence voltage components into the three-phase modulation signals to change the duty cycle of state "O." First, the compensation zero-sequence voltage calculation method of the proposed method is introduced. In addition, a controller is designed to achieve closed-loop control of the neutral-point potential.

The basic principles

The proposed NPV balancing method includes two key procedures:

1. Inject the zero-sequence components u_0.

To improve the utilization rate of DC-link voltage, a zero-sequence component is injected into the original three-phase modulation signals. The zero-sequence voltage is designed as Equation 2:

$$u_0 = \text{mid}\{u_a, u_b, u_c\}/2 \qquad (2)$$

where u_a, u_b, and u_c indicate the original three-phase modulation signals.

The obtained three-phase reference voltage can be expressed as Equation 3:

$$\begin{cases} u_a^* = u_a + u_0 \\ u_b^* = u_b + u_0 \\ u_c^* = u_c + u_0 \end{cases} \qquad (3)$$

1. Calculate $u_{max}, u_{mid}, u_{min}$ and $i_{u\,max}, i_{u\,mid}, i_{u\,min}$.

$u_{max}, u_{mid}, u_{min}$ represent the maximum, medium, and minimum values of the three-phase reference voltage, respectively, $i_{u\,max}$ is the instantaneous value of the phase current corresponding to the maximum value of the three-phase reference voltage, $i_{u\,mid}$ is the instantaneous value of the phase current corresponding to the medium value of the three-phase reference voltage, and $i_{u\,min}$ is the instantaneous value of the phase current corresponding to the minimum value of the three-phase reference voltage.

$u_{max}, u_{mid}, u_{min}$ are expressed as Equation 4:

$$\begin{cases} u_{max} = u_l^* = \max\{u_a^*, u_b^*, u_c^*\} & l \in (a, b, c) \\ u_{mid} = u_m^* = \text{mid}\{u_a^*, u_b^*, u_c^*\} & m \in (a, b, c) \\ u_{min} = u_n^* = \min\{u_a^*, u_b^*, u_c^*\} & n \in (a, b, c) \end{cases} \qquad (4)$$

$i_{u\,max}, i_{u\,mid}, i_{u\,min}$ are expressed as Equation 5:

$$\begin{cases} i_{u\,max} = i_l & l \in (a, b, c) \\ i_{u\,mid} = i_m & m \in (a, b, c) \\ i_{u\,min} = i_n & n \in (a, b, c) \end{cases} \qquad (5)$$

1. Calculate the compensated zero-sequence voltage u_{com}.

According to the proposed neutral-point potential compensation strategy in this article, calculate the required compensation zero-sequence component and inject it into the three-phase reference voltage modulation signals to achieve control of neutral-point potential balance. The final modulation voltage is expressed as Equation 6:

$$\begin{cases} u_{max}^* = u_{max} + u_{com} \\ u_{mid}^* = u_{mid} + u_{com} \\ u_{min}^* = u_{min} + u_{com} \end{cases} \qquad (6)$$

Duty cycle calculations

The calculation of the duty cycles varies under different carrier modulation strategies. This section derives the PD-PWM as an example. Under the PD-PWM modulation strategy, the modified modulation signals within each switching period exhibit the following four situations based on their amplitude, as shown in Figure 2.

When $u_x^* \geq 0, (x = max, mid, min)$, the duty cycle of the "P" and "O" states is expressed as Equations 7, 8:

$$d_{xP} = u_x^*/u_1 \qquad (7)$$

$$d_{xO} = 1 - u_x^*/u_1 \qquad (8)$$

When $u_x^* < 0, (x = max, mid, min)$, the duty cycle of the "N" and "O" states is expressed as Equations 9, 10:

$$d_{xN} = |u_x^*|/u_2 = -u_x^*/u_2 \qquad (9)$$

$$d_{xO} = 1 + u_x^*/u_2 \qquad (10)$$

Normalize the compensated modulation signals, and the corresponding duty cycles are expressed as Equation 11:

$$\begin{cases} \begin{cases} d_{maxP} = u_{max}^*/u_1 = (u_{max} + u_{com})/u_1 & (u_{max}^* \geq 0) \\ d_{maxN} = -u_{max}^*/u_2 = -(u_{max} + u_{com})/u_2 & (u_{max}^* < 0) \end{cases} \\ \begin{cases} d_{midP} = u_{mid}^*/u_1 = (u_{mid} + u_{com})/u_1 & (u_{mid}^* \geq 0) \\ d_{midN} = -u_{mid}^*/u_2 = -(u_{mid} + u_{com})/u_2 & (u_{mid}^* < 0) \end{cases} \\ \begin{cases} d_{minP} = u_{min}^*/u_1 = (u_{min} + u_{com})/u_1 & (u_{min}^* \geq 0) \\ d_{minN} = -u_{min}^*/u_2 = -(u_{min} + u_{com})/u_2 & (u_{min}^* < 0) \end{cases} \end{cases} \qquad (11)$$

where subscripts "P" and "N" indicate the output voltage state.

The compensated zero-sequence voltage

The averaged neutral-point current within a modulation period is expressed as Equation 12:

$$\overline{i_o} = \sum_{i=a,b,c} d_{io} i_i = \sum_{i=a,b,c} (1 - d_{iP} - d_{iN}) i_i = \sum_{i=a,b,c} \left(1 - \frac{|u_i^*|}{V_{dc}/2}\right) i_i \qquad (12)$$

It can be observed that adjusting the compensated modulated signal u_x^* can alter the duty cycle of the state "O" d_{io}. Because the controlled component of the compensated modulated signal u_x^* solely consists of the compensated zero-sequence voltage component u_{com}, it can be concluded that changing u_{com} can modify the duty cycle of the state "O," thereby achieving control over the averaged neutral-point current and ultimately suppressing neutral-point potential fluctuations.

The averaged neutral-point current corresponding to the four types of modified modulation signals is analyzed as Equations 13–16:
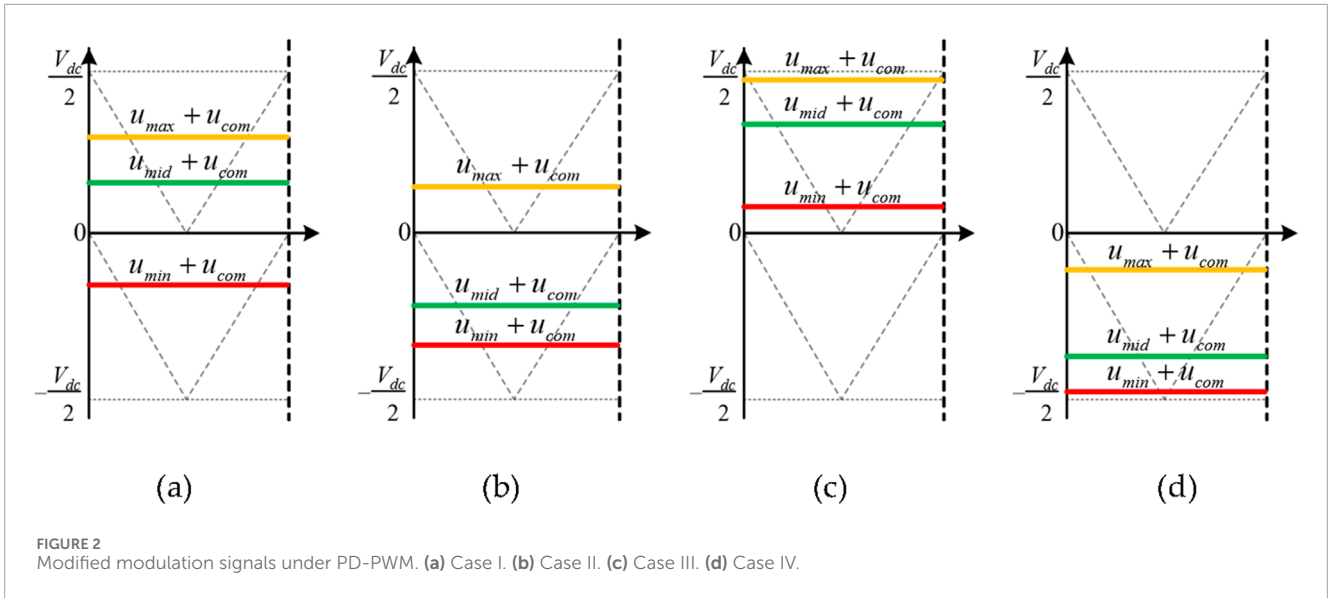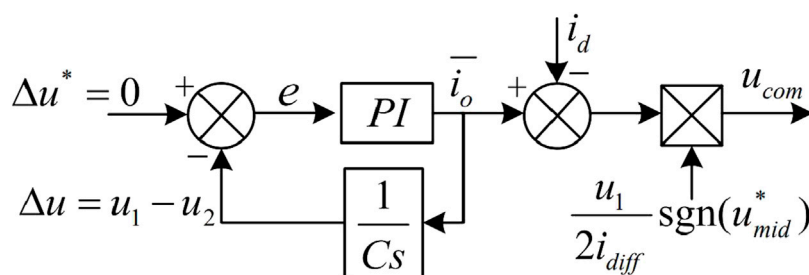
FIGURE 2
Modified modulation signals under PD-PWM. **(a)** Case I. **(b)** Case II. **(c)** Case III. **(d)** Case IV.

TABLE 1 The averaged neutral-point current under different situations.

The modulation voltages and compensated zero-sequence voltage	The averaged neutral-point current
$u_a^* > 0, u_b^* < 0, u_c^* < 0; -u_a^* < u_{com} < -\min\{u_b^*, u_c^*\}$	$2\left(-u_a^* i_a + u_b^* i_b + u_c^* i_c\right)/V_{dc} - 4u_{com} i_a/V_{dc}$
$u_a^* > 0, u_b^* > 0, u_c^* < 0; -\max\{u_a^*, u_b^*\} < u_{com} < -u_c^*$	$2\left(-u_a^* i_a - u_b^* i_b + u_c^* i_c\right)/V_{dc} + 4u_{com} i_c/V_{dc}$
$u_a^* < 0, u_b^* > 0, u_c^* < 0; -u_b^* < u_{com} < -\min\{u_a^*, u_c^*\}$	$2\left(u_a^* i_a - u_b^* i_b + u_c^* i_c\right)/V_{dc} - 4u_{com} i_b/V_{dc}$
$u_a^* < 0, u_b^* > 0, u_c^* > 0; -\max\{u_b^*, u_c^*\} < u_{com} < -u_a^*$	$2\left(u_a^* i_a - u_b^* i_b - u_c^* i_c\right)/V_{dc} + 4u_{com} i_a/V_{dc}$
$u_a^* < 0, u_b^* < 0, u_c^* > 0; -u_c^* < u_{com} < -\min\{u_a^*, u_b^*\}$	$2\left(u_a^* i_a + u_b^* i_b - u_c^* i_c\right)/V_{dc} - 4u_{com} i_c/V_{dc}$
$u_a^* > 0, u_b^* < 0, u_c^* > 0; -\max\{u_a^*, u_c^*\} < u_{com} < -u_b^*$	$2\left(-u_a^* i_a + u_b^* i_b - u_c^* i_c\right)/V_{dc} + 4u_{com} i_b/V_{dc}$

FIGURE 3
Control block diagram for compensating zero-sequence component.

1. Case I: $u_{max}^* > 0, u_{mid}^* \geq 0, u_{min}^* \leq 0$

$$\begin{aligned}
\bar{i}_o &= \left(1 - d_{max\ P}\right)i_{u\,max} + \left(1 - d_{mid\ P}\right)i_{u\,mid} + \left(1 - d_{minN}\right)i_{u\,min} \\
&= \frac{1}{u_1}\left(-u_{max}i_{u\,max} - u_{mid}i_{u\,mid} + u_{min}i_{u\,min}\right) + \frac{u_{com}}{u_1}\left(-i_{u\,max} - i_{u\,mid} + i_{u\,min}\right) \\
&= i_{d1} + 2\frac{u_{com}}{u_1}i_{u\,min}
\end{aligned}$$

(13)

2. Case II: $u_{max}^* \geq 0, u_{mid}^* \leq 0, u_{min}^* < 0$

$$\begin{aligned}
\bar{i}_o &= \left(1 - d_{max\ P}\right)i_{u\,max} + \left(1 - d_{mid\ N}\right)i_{u\,mid} + \left(1 - d_{minN}\right)i_{u\,min} \\
&= \frac{1}{u_1}\left(-u_{max}i_{u\,max} + u_{mid}i_{u\,mid} + u_{min}i_{u\,min}\right) + \frac{u_{com}}{u_1}\left(-i_{u\,max} + i_{u\,mid} + i_{u\,min}\right) \\
&= i_{d2} - 2\frac{u_{com}}{u_1}i_{u\,max}
\end{aligned}$$

(14)

TABLE 2 The required compensation zero-sequence component and phase current sign relationship for different neutral-point potential fluctuations.

Δu	$\overline{i_o}$	i_{diff}		u_{com}
		$u_{mid}^* \geq 0$	$u_{mid}^* < 0$	
$u_1 \geq u_2 \Delta u \geq 0$	$\overline{i_o} \geq 0$	$i_{u\,min} < 0$	$i_{u\,max} \geq 0$	$u_{com} \leq 0$
$u_1 < u_2 \Delta u < 0$	$\overline{i_o} < 0$			$u_{com} > 0$

TABLE 3 Parameters of the experimental setup.

Parameters	Value	Parameters	Value
Output power	5 kW	DC-link capacitor	2200 μF
Grid phase voltage (RMS)	220 V	Unbalanced capacitor	840 μF
Grid frequency	50 Hz	Unbalanced resistance	100 kΩ, 50 kΩ
Switching frequency	20 kHz	Filter inductor	3 mH


```
Original three-phase modulation voltage
            ↓ uₐ、ub、uc
Inject zero-sequence
components uₒ according to (2)
            ↓
Calculate umax, umid, umin and i_u max,
i_u mid, i_u min according to (4),(5)
            ↓
Calculate ucom and the final three-
phase modulation voltage
according to (23),(6)
```
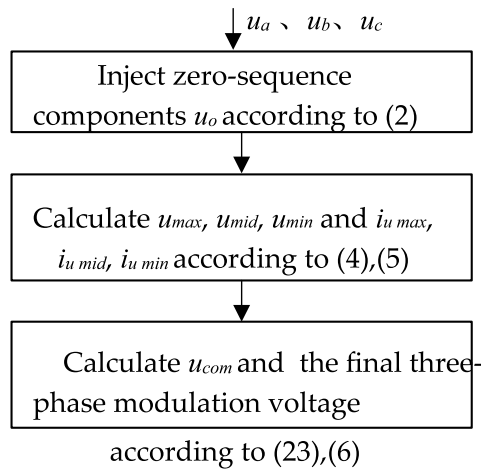
FIGURE 4
Flow chart of the proposed neutral-point voltage balancing method.

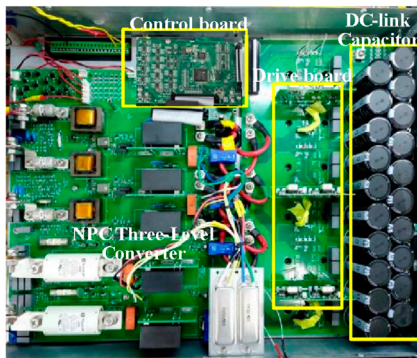

FIGURE 5
Experimental setup of 3L-NPC converters.

3. Case III: $u_{max}^* > 0, u_{mid}^* > 0, u_{min}^* \geq 0$

$$\overline{i_o} = (1 - d_{maxP})i_{u\,max} + (1 - d_{mid\,P})i_{u\,mid} + (1 - d_{min\,P})i_{u\,min}$$
$$= \frac{1}{u_1}\left(-u_{max}i_{u\,max} - u_{mid}i_{u\,mid} - u_{min}i_{u\,min}\right) - \frac{u_{com}}{u_1}\left(i_{u\,max} + i_{u\,mid} + i_{u\,min}\right) = i_{d3} \quad (15)$$

4. Case IV: $u_{max}^* \leq 0, u_{mid}^* < 0, u_{min}^* < 0$

$$\overline{i_o} = (1 - d_{maxP})i_{u\,max} + (1 - d_{mid\,P})i_{u\,mid} + (1 - d_{min\,P})i_{u\,min}$$
$$= \frac{1}{u_1}\left(u_{max}i_{u\,max} + u_{mid}i_{u\,mid} + u_{min}i_{u\,min}\right) + \frac{u_{com}}{u_1}\left(i_{u\,max} + i_{u\,mid} + i_{u\,min}\right) = i_{d4} \quad (16)$$

where i_{d1}, i_{d2}, i_{d3}, and i_{d4} are the neutral-point fluctuation currents.

The analysis reveals that the averaged neutral-point current contains compensated zero-sequence components when the compensated modulation signal is as shown in Figure 2 in Case I and Case II. The signs of three-phase modulation signals are not the same, which means that the averaged neutral-point current can be compensated and controlled by changing the compensating zero-sequence component, thereby controlling the neutral-point potential. When the compensated modulation signal is in Case III and Case IV, as shown in Figure 2, the signs of the three-phase modulation signals are the same, and the averaged neutral-point current does not contain the compensated zero-sequence component. This indicates that injecting zero-sequence components does not affect the averaged neutral-point current, thus making it impossible to control the neutral-point potential. Therefore, when using the compensation zero-sequence component injection to achieve balanced control of neutral-point potential, it is necessary to avoid the situation where the modulation signals maintain consistent polarity after injecting the zero-sequence component.

The averaged neutral-point current after injecting the compensating zero-sequence component is expressed as Equation 17:

$$\overline{i_o} = \left(1 - \frac{|u_a^* + u_{com}|}{V_{dc}/2}\right)i_a + \left(1 - \frac{|u_b^* + u_{com}|}{V_{dc}/2}\right)i_b + \left(1 - \frac{|u_c^* + u_{com}|}{V_{dc}/2}\right)i_c \quad (17)$$

Assume that $u_a^* > 0, u_b^* < 0, u_c^* < 0$ and $-u_a^* < u_{com} < \max\{u_b^*, u_c^*\}$, Equation 17 can be expressed as Equation 18:

$$\overline{i_o} = (i_a + i_b + i_c) + \frac{2}{V_{dc}}\left(-u_a^* i_a + u_b^* i_b + u_c^* i_c\right) + \frac{2u_{com}}{V_{dc}}\left(-i_a + i_b + i_c\right) = i_d + i_{com} \quad (18)$$

According to (18), there are three parts included in the averaged neutral-point current: 1) The sum of the grid side currents. This component is zero in a three-phase three-line system. 2) The second part is the neutral-point fluctuation current generated by the PD-PWM modulation strategy, represented as i_d. This item is uncontrollable and the fundamental cause of neutral-point potential
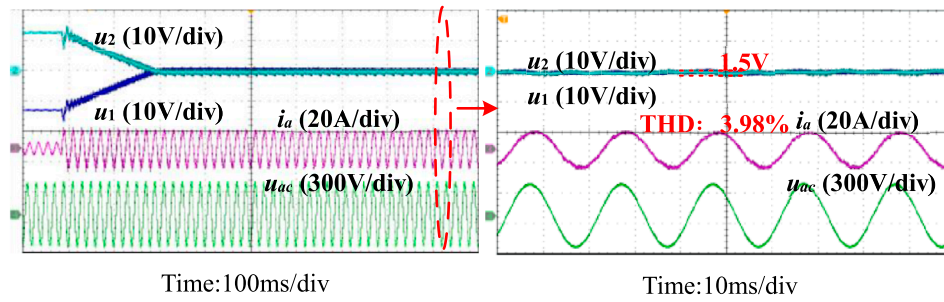
FIGURE 6
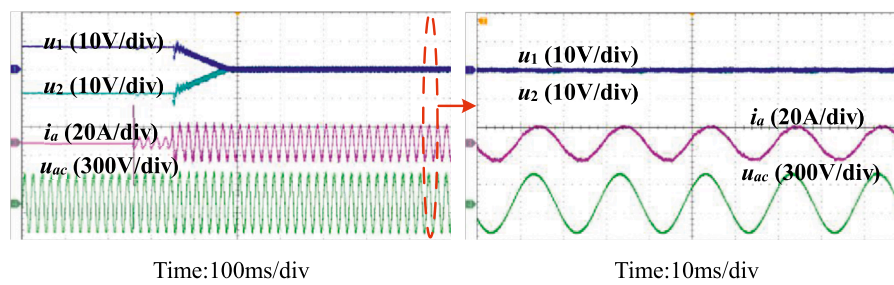Experimental results under an unbalanced capacitance condition.

FIGURE 7
Experimental results of an unbalanced equivalent leakage current condition.
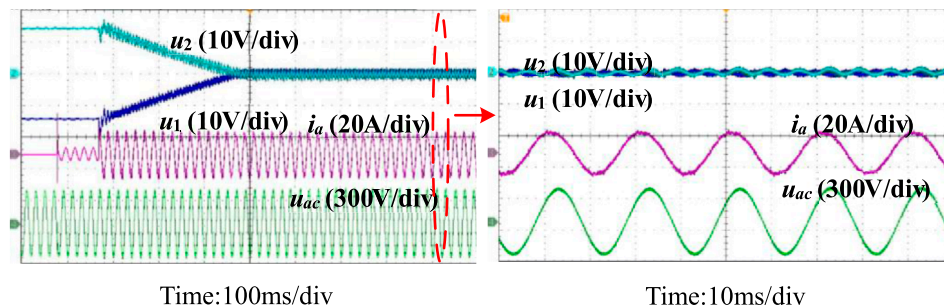

FIGURE 8
Experimental results of the proposed method under unbalanced capacitance with a power factor of 0.7.

fluctuations. 3) The third part is the compensation current generated by injecting the zero-sequence component, represented as i_{com}. The proposed method utilizes icom to compensate for the neutral-point fluctuation current id, thereby controlling the averaged neutral-point current.

The averaged neutral-point current for other modulation voltages and compensated zero-sequence voltages can be derived similarly. Therefore, the averaged neutral-point current under different situations is summarized in Table 1.

To avoid the situation where the modulation signals maintain the same polarity after injecting the zero-sequence component, the compensation voltage must meet Equation 19:

$$-\max\left(u_i^*\right) < u_{com} < -\min\left(u_i^*\right) \tag{19}$$

According to Equations 13, 14, it can be seen that the expression of the compensating zero-sequence component is related to the sign of u_{mid}^* and can be expressed as follows:

1. When $u_{mid}^* \geq 0$, the compensation zero-sequence component is derived as Equation 20:

$$u_{com} = \left(\overline{i_o} - i_{d1}\right)\frac{u_1}{2i_{u\,min}} \tag{20}$$

2. When $u_{mid}^* < 0$, the compensation zero-sequence component is derived as Equation 21:

TABLE 4 Comparison of the existing methods and the proposed method.

Method	Zero-sequence voltage injection (Wang et al., 2016)	Model predictive control (Alhosaini et ; 2021)	Proposed method
Computational burden	High	High	Medium
Parameter dependency	Yes	No	No

$$u_{com} = \left(\overline{i_o} - i_{d2} \right) \frac{u_1}{-2i_{u\ max}} \tag{21}$$

Therefore, the control block diagram of the compensation zero-sequence component is designed as shown in Figure 3.

Where i_{diff} is the phase current whose polarity is different from that of the other two phases, $\Delta u = u_1 - u_2$ is neutral-point potential fluctuation, sgn() is the sign function, and i_d is the unified expression for the neutral-point fluctuation current, expressed as Equation 22:

$$i_d = i_{d1} \frac{\text{sgn}\left(u_{mid}^*\right) + 1}{2} + i_{d2} \frac{\text{sgn}\left(u_{mid}^*\right) - 1}{-2} \tag{22}$$

The required compensation zero-sequence component and phase current sign relationship for different neutral-point potential fluctuations are shown in Table 2. It can be concluded that the sign of the compensating zero-sequence component is related to the fluctuation of neutral-point potential and the sign of the phase current involved in generating the compensating neutral-point current. From the above derivation, the sign of the modulation signal after adding the compensating zero-sequence component determines the phase current used to generate the compensating neutral-point current. Therefore, the sign of the required compensating zero-sequence component can be obtained.

Therefore, the expression for the compensation zero-sequence component can be obtained as Equation 23:

$$u_{com} = -k_p \left(1 + \frac{k_i}{s} \right) \cdot |\Delta u| \cdot \text{sgn}(\Delta u \cdot i_{u\ min}) \tag{23}$$

where k_p and k_i are the proportional coefficient and integral coefficient of the proportional-integral (PI) controller, respectively.

In summary, the flow chart of the proposed neutral-point voltage balancing method is shown in Figure 4.

Discussion

The experimental prototype of the 3L-NPC converter is shown in Figure 5, and the main parameters are listed in Table 3.

The experimental results of the proposed control method under unbalanced capacitance are shown in Figure 6. The experimental results showed that when there is a difference in

the DC-link capacitance of the inverter, the proposed neutral-point potential balance control method can effectively balance the neutral-point potential. The corresponding total harmonic distortion (THD) values of the currents are 3.98%. The THD is smaller than 5%, which meets IEEE Std. 519-2014. The DC capacitor voltage ripple is less than 1.5 V in the steady state, indicating that the proposed method has good steady-state performance.

Figure 7 shows the experimental waveforms under unbalanced equivalent leakage current (unbalanced parallel resistance simulates unbalanced equivalent leakage current). The experimental results showed that when there is a difference in the equivalent leakage current of the DC-link capacitors, the presented method can also effectively balance the neutral-point potential.

Figure 8 shows the experimental results of the proposed method under unbalanced capacitance and with a power factor of 0.7. It can be observed that after applying the proposed neutral-point potential balance control method, even when the inverter operates at a non-unity power factor, it can effectively balance the neutral-point potential caused by the difference in DC-link capacitance.

A comparison between the proposed method and other existing methods is shown in Table 4. The zero-sequence voltage injection method based on modulation wave decomposition involves the calculation of many trigonometric functions. The model predictive control (MPC) method based on virtual space vectors requires the calculation of a cost function, which has strong parameter dependence, which is not expected in practical applications. In addition, the MPC method involves the selection of weight factors. In contrast, the proposed method has a relatively smaller computational burden and is not dependent on circuit parameters.

Conclusion

This article proposes a neutral-point potential balance control method based on zero-sequence component injection to address the issue of neutral-point potential imbalance in 3L-NPC converters. The basic principle and the compensation zero-sequence voltage calculation of the method are introduced. Based on the relationship between the averaged neutral-point current and the neutral-point potential, a neutral-point potential balance controller is designed. Finally, a 3L-NPC converter prototype is developed to verify the feasibility of the proposed neutral-point potential balance control method under the conditions of unbalanced DC-link capacitance and unbalanced equivalent leakage current. The experimental results show that the developed control method can effectively balance the neutral-point potential with hardware differences under different operating conditions, ensuring safe and stable operation of the system.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material; further inquiries can be directed to the corresponding author.

Author contributions

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Conflict of interest

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References

Alhosaini, W., Diao., F., Mahmud, M. H., Wu, Y., and Zhao, Y. (2021). A virtual space vector-based model predictive control for inherent DC-Link voltage balancing of three-level T-Type converters. *IEEE J. Emerg. Sel. Top. Power Electron.* 9, 1751–1764. doi:10.1109/jestpe.2020.3002192

Alsofyani, I. M., and Lee, K.-B. (2021). Simple capacitor voltage balancing for three-level NPC inverter using discontinuous PWM method with hysteresis neutral-point error band. *IEEE Trans. Power Electron.* 36, 12490–12503. doi:10.1109/tpel.2021.3074957

Chen, F., Qiao, W., Wang, H., and Qu, L. A. (2021). A simple zero-sequence voltage injection method for carrier-based pulsewidth modulation of the three-level NPC inverter. *IEEE J. Emerg. Sel. Top. Power Electron.* 9, 4687–4699. doi:10.1109/jestpe.2020.3012726

Giri, S.Kr., Chakrabarti, S., Banerjee, S., and Chakraborty, C. (2017). A carrier-based PWM scheme for neutral point voltage balancing in three-level inverter extending to full power factor range. *IEEE Trans. Ind. Electron.* 64, 1873–1883. doi:10.1109/tie.2016.2624721

Giri, S. K., Banerjee, S., and Chakraborty, C. (2019). An improved modulation strategy for fast capacitor voltage balancing of three-level NPC inverters. *IEEE Trans. Ind. Electron.* 66, 7498–7509. doi:10.1109/tie.2018.2880723

Guo, F., Yang, T., Li, C., Bozhko, S., and Wheeler, P. (2022). Active modulation strategy for capacitor voltage balancing of three-level neutral-point-clamped converters in high-speed drives. *IEEE Trans. Ind. Electron.* 69, 2276–2287. doi:10.1109/tie.2021.3065605

Jiang, W., Wang, P., Ma, M., Wang, J., Li, J., Li, L., et al. (2020). A novel virtual space vector modulation with reduced common-mode voltage and eliminated neutral point voltage oscillation for neutral point clamped three-level inverter. *IEEE Trans. Ind. Electron.* 67, 884–894. doi:10.1109/tie.2019.2899564

Lee, D.-J., Choi, J.-H., and Choi, U.-M. (2025). Reliability improved discontinuous pulse width modulation for NPC inverters operated at high modulation index. *IEEE Trans. Power Electron.* 40, 9876–9888. doi:10.1109/tpel.2025.3547374

Lewicki, A., Kondratenko, D., and Odeh, C. I. (2024). Hybridized PWM strategy for Three- and multiphase three-level NPC inverters. *IEEE Trans. Ind. Electron.* 71, 8279–8290. doi:10.1109/tie.2023.3321999

Li, K., Wei, M., Xie, C., Deng, F., Guerrero, J. M., and Vasquez, J. C. (2018). Triangle carrier-based DPWM for three-level NPC inverters. *IEEE J. Emerg. Sel. Top. Power Electron.* 6, 1966–1978. doi:10.1109/jestpe.2018.2812704

Liu, G., Wang, D., Wang, M., Zhu, C., and Wang, M. (2018). Neutral-point voltage balancing in three-level inverters using an optimized virtual space vector PWM with reduced commutations. *IEEE Trans. Ind. Electron.* 65, 6959–6969. doi:10.1109/tie.2018.2798565

Mukherjee., S., Giri, S. K., and Banerjee, S. (2019). A flexible discontinuous modulation scheme with hybrid capacitor voltage balancing strategy for three-level NPC traction inverter. *IEEE Trans. Industrial Electron.* 66, 3333–3343. doi:10.1109/tie.2018.2851967

Rivera, S., Wu, B., Kouro, S., Yaramasu, V., and Wang, J. (2015). Electric vehicle charging station using a neutral point clamped converter with bipolar DC bus. *IEEE Trans. Ind. Electron.* 62, 1999–2009. doi:10.1109/tie.2014.2348937

Sarker, R., Bhattacharya, A., Debnath, S., Castillo-Atoche, A., and Datta, A. (2024). A novel FPGA-driven HD-SPWM architecture with zero-sequence voltage insertion strategy for three-level NPC inverter. *IEEE Trans. Ind. Inf.* 20, 10814–10824. doi:10.1109/tii.2024.3393566

Von Jouanne, A., Dai, S., and Zhang, H. A. (2002). A multilevel inverter approach providing DC-link balancing, ride-through enhancement, and common-mode voltage elimination. *IEEE Trans. Ind. Electron.* 49, 739–745. doi:10.1109/tie.2002.801233

Wan., W., Duan, S., Chen, C., and Yu, T. (2021). A hybrid control method for neutral-point voltage balancing in three-level inverters. *IEEE Trans. Power Electron.* 36, 8575–8582. doi:10.1109/tpel.2021.3051044

Wang, Z., Cui, F., Zhang, G., Shi, T., and Xia, C. (2016). Novel carrier-based PWM strategy with zero-sequence voltage injected for three-level NPC inverter. *IEEE J. Emerg. Sel. Top. Power Electron.* 4, 1442–1451. doi:10.1109/jestpe.2016.2591618

Wang, J., Yuan, X., Dagan, K. J., and Bloor, A. (2020). Optimal neutral-point voltage balancing algorithm for three-phase three-level converters with hybrid zero-sequence signal injection and virtual zero-level modulation. *IEEE Trans. Industry Appl.* 56, 3865–3878. doi:10.1109/tia.2020.2983659

Yamanaka, K., Hava, A. M., Kirino, H., Tanaka, Y., Koga, N., and Kume, T. (2002). A novel neutral point potential stabilization technique using the information of output current polarities and voltage vector. *IEEE Trans. Ind. Appl.* 38, 1572–1580. doi:10.1109/tia.2002.804761

Zhang., Y., Li., J., Li., X., Cao, Y., Sumner., M., and Xia, C. (2017). A method for the suppression of fluctuations in the neutral-point potential of a three-level NPC inverter with a capacitor-voltage loop. *IEEE Trans. Power Electron.* 32, 825–836. doi:10.1109/tpel.2016.2536176