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Discrete-time deadbeat control for STATCOMs based on dq reference frame: a high-speed, tuning-free strategy for reactive current regulation

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The increasing penetration of distributed generation and the evolving requirements of smart grids have heightened the demand for fast, accurate, and robust reactive power control in Static Synchronous Compensators (STATCOMs). While proportional-integral (PI) controllers remain widely adopted, their reliance on iterative tuning and limited performance under low switching frequencies restricts their application in modern high-voltage cascaded H-bridge (CHB) systems. This paper proposes a novel discrete-time deadbeat current control method formulated directly in the synchronous rotating dq reference frame. By transforming AC currents into DC signals, the control structure is simplified and enables precise decoupled regulation of active and reactive currents. Unlike conventional approaches that discretize analog-domain designs, the proposed controller is derived analytically in the discrete domain, eliminating the need for parameter tuning or empirical adjustment. Simulation studies confirm that the approach achieves excellent current tracking accuracy, robust performance under $\pm 10\%$ inductance and -10% to $+40\%$ resistance variations, and maintains low total harmonic distortion even at low switching frequencies. These features make the method particularly suitable for high-voltage cascaded H-bridge STATCOM applications. Furthermore, stability analysis demonstrates that the closed-loop poles remain inside the unit circle across parameter deviations, ensuring reliable operation. The results indicate that the proposed approach provides a practical, fully digital control solution that improves accuracy, robustness, and implementation efficiency in modern smart grid environments.

KEYWORDS

static synchronous compensator, deadbeat control, cascaded H-bridge, discrete-time control, dq reference frame, reactive power compensation, total harmonic distortion

1 Introduction

As a critical device in Flexible AC Transmission Systems (FACTS), the Static Synchronous Compensator (STATCOM) has been extensively and deeply applied

in modern power systems due to its superior performance (Zhong, 2020). With the rapid development of renewable energies, power generation fluctuation issues have become increasingly prominent. STATCOMs, with their fast and accurate reactive power regulation capabilities, play a pivotal role in maintaining grid stability (Pereira et al., 2011). They significantly enhance voltage quality and system stability, providing reliable support for efficient grid integration of clean energy (Kroposki et al., 2010). The response speed of STATCOM to changes in reactive power demand is crucial, typically requiring regulation within a single fundamental cycle to ensure stable operation. The performance of the current regulator directly affects reactive current output, making it a core component in reactive power compensation.

In practical applications, STATCOMs are controlled using digital controllers. The conventional PI control strategy involves designing the controller in the continuous domain, followed by discretization for digital implementation. Due to the inevitable time delays in digital processing, a one-step delay in control output is usually adopted to avoid constraints on PWM duty cycles (Shan et al., 2009). However, this delay introduces phase lag, which reduces the phase margin of the closed-loop system and negatively affects stability (Yang, 2015). Furthermore, selecting an appropriate PI controller bandwidth and mitigating the influence of the delay are major challenges in achieving both fast response and high steady-state accuracy.

Deadbeat control is a control strategy specifically designed for discrete-time systems and can be effectively implemented in digital controllers. It offers the fastest possible response (minimum steps) with zero steady-state error (Kawamura et al., 1988). In the discrete domain, the one-step delay can be incorporated into the plant model, whereas in the continuous domain it requires complex approximations like Padé approximation (Ellis, 2004). Although some deadbeat control methods for STATCOM exist, most are designed in stationary reference frames (Camargo et al., 2020; Chen et al., 2015). In these frameworks, the current reference signal is sinusoidal, making it difficult to eliminate steady-state error despite achieving fast tracking. This is because existing methods primarily focus on pole placement for fast response, neglecting the characteristics of the input signal (Luo et al., 2015). Recent advances in predictive and repetitive controllers offer alternatives, but they typically involve high computational effort and iterative prediction, which hinder their practical deployment in high-power STATCOM systems.

To address these limitations, this paper proposes a deadbeat current control method for STATCOM based on the dq rotating reference frame. The main contributions are as follows:

- By transforming AC quantities to DC quantities using synchronous rotating coordinates and designing the controller in the discrete domain, the method achieves fast response and zero steady-state error. It also offers strong tracking and parameter adaptation capabilities, providing an effective solution for STATCOM current control.
- Unlike conventional PI control, this method avoids frequency characteristic distortion during the discretization process and maintains more stable control performance under low-frequency conditions.

- Differing from existing deadbeat methods based on stationary coordinates, this approach uses step signals in the dq frame as references, enabling truly zero steady-state error control.

The proposed method offers a novel and effective approach to STATCOM current control, characterized by fast dynamics, high steady-state accuracy, and strong parameter adaptability—enhancing the control performance of STATCOMs and supporting power system stability.

The paper is organized as follows: Section 2 analyzes the STATCOM model in dq reference frame; Section 3 presents the control sequence and algorithm design of the deadbeat controller; Section 4 validates the method's performance through simulation and robustness analysis; and Section 5 concludes the paper with major findings and outcomes.

2 System model of STATCOM in dq reference frame

This study focuses on a star-connected Cascaded H-Bridge (CHB) STATCOM circuit topology, as shown in Figure 1. The device consists of three identical phase circuits, with each phase connected to a 35 kV power grid through a filter inductor L . The same number of H-bridge modules are cascaded in each phase, using Carrier Phase-Shifted Pulse Width Modulation (CPS-PWM) for switching control. This reduces the voltage stress on individual devices and ensures high-quality output voltage waveforms.

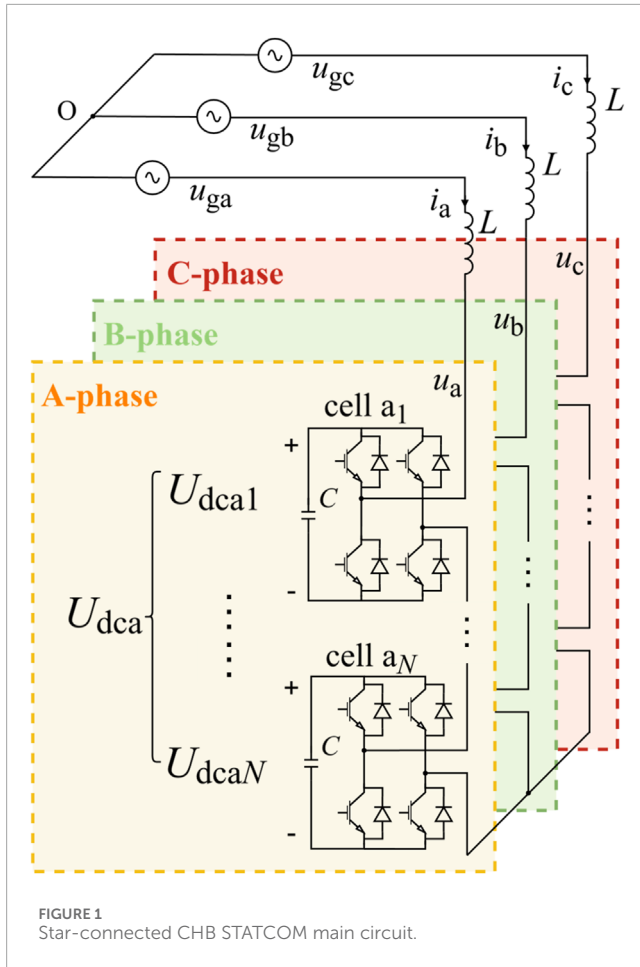
Each H-bridge module contains an independent floating capacitor C . u_{gk} ($k = a, b, c$) is the three-phase grid voltage, u_k is the STATCOM three-phase output voltage, i_k is the three-phase current, U_{dck} is the average DC voltage per phase leg, U_{dckj} ($j = 1, 2, \dots, N$) is the DC voltage of a single H-bridge in one phase, and N is the number of modules. The STATCOM is connected in parallel to the grid with the load. Its operating principle is to control its output voltage to regulate the amplitude and phase of the grid-connected current, thereby achieving dynamic reactive power compensation, as indicated in Figure 2.

Ideally, there is no active power exchange between STATCOM and the grid. The output voltage vector $\vec{U}_c$ remains in phase with the grid voltage vector $\vec{U}_g$ via a Phase-Locked Loop (PLL). When the STATCOM output voltage u_c exceeds the grid voltage u_g , the current leads the grid voltage by 90° , and STATCOM operates in a capacitive mode, as shown in Figure 2A. Conversely, when the output voltage is lower than the grid voltage, the current lags the voltage by 90° , indicating inductive operation as shown in Figure 2B. This study focuses on current control of CHB STATCOMs. The balancing of DC capacitor voltages is not discussed herein and refers to (Akagi et al., 2007; Shen, 2021).

Let the grid voltage magnitude be U_g and its instantaneous value expressed in Equation 1:

$$\begin{cases} u_{ga} = U_g \cos(\omega t) \\ u_{gb} = U_g \cos(\omega t - 2\pi/3) \\ u_{gc} = U_g \cos(\omega t + 2\pi/3) \end{cases} \quad (1)$$

According to the



the inductor equivalent resistance R , the voltage balance equation is shown in Equation 2:

$$L \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} u_{ga} \\ u_{gb} \\ u_{gc} \end{bmatrix} - \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} - R \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (2)$$

Applying the synchronous rotating dq transformation yields the time-domain model of the STATCOM plant in the dq frame:

$$L \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -R & \omega L \\ -\omega L & -R \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} u_{gd} - u_d \\ u_{gq} - u_q \end{bmatrix} \quad (3)$$

Where u_d , u_q , i_d and i_q are the d- and q-axis components of the STATCOM output voltage and current in the rotating reference frame, respectively; ω denotes the angular velocity of the synchronous rotating frame; u_{gd} and u_{gq} are the d- and q-axis components of the grid voltage. By applying the Laplace transform to Equation 3, the frequency-domain model of the STATCOM plant is obtained obtained in Equation 4 as follows:

$$sL \begin{bmatrix} I_d(s) \\ I_q(s) \end{bmatrix} = \begin{bmatrix} -R & \omega L \\ -\omega L & -R \end{bmatrix} \begin{bmatrix} I_d(s) \\ I_q(s) \end{bmatrix} + \begin{bmatrix} U_{gd}(s) - U_d(s) \\ U_{gq}(s) - U_q(s) \end{bmatrix} \quad (4)$$

Where $I_d(s)$ and $I_q(s)$ represent the d- and q-axis components of the STATCOM current in the frequency domain, while $U_d(s)$

and $U_q(s)$ denote the corresponding voltage components. Similarly, $U_{gd}(s)$ and $U_{gq}(s)$ are the d- and q-axis components of the grid voltage in the frequency domain. The plant model of the STATCOM in the dq reference frame is illustrated in Figure 3.

According to instantaneous power theory (Akagi et al., 2017a; Akagi et al., 2017b), the instantaneous active and reactive powers drawn from the grid are shown in Equation 5:

$$\begin{cases} p = u_{gd}i_d + u_{gq}i_q = u_{gd}i_d \\ q = u_{gq}i_d - u_{gd}i_q = -u_{gd}i_q \end{cases} \quad (5)$$

With the d-axis aligned with the grid voltage vector, q-axis voltage component $u_{gq} = 0$. Thus, active and reactive power can be independently regulated by adjusting i_d and i_q .

The control of active and reactive currents i_d and i_q is implemented using a closed-loop scheme. To eliminate the inherent coupling between active and reactive components in the plant model (as shown in Figure 3), and to mitigate the influence of grid voltage disturbances, current decoupling and voltage feedforward compensation are incorporated into the STATCOM controller, as illustrated in Figure 4. Essentially, the STATCOM operates as a voltage source for grid-connected current control. In Figure 4, $G_{id}(s)$ and $G_{iq}(s)$ represent the transfer functions of the active and reactive current regulators, respectively; I_{dref} and I_{qref} are the reference values for active and reactive currents, and i_d and i_q are the d- and q-axis components of the measured three-phase current after dq transformation.

By treating the coordinate transformation processes as unity gain elements and canceling the coupling paths between the controller and the plant, Figures 3, 4 can be combined and simplified into the equivalent control system structure shown in Figure 5, which represents active and reactive current control in the dq reference frame. The control structures for both active and reactive currents are identical, and the plant is modeled as a first-order low-pass system composed of the filter inductance and its equivalent resistance.

As shown in Figure 5, the simplified control structure reveals that both active and reactive current controllers operate over identical low-pass plant models, facilitating a unified control design strategy.

Conventional designs of $G_{id}(s)$ and $G_{iq}(s)$ typically employ PI regulators, with detailed design procedures provided in (Shan et al., 2009). In contrast, this paper proposes an alternative approach based on deadbeat control, which not only achieves superior current regulation performance but also significantly simplifies the digital

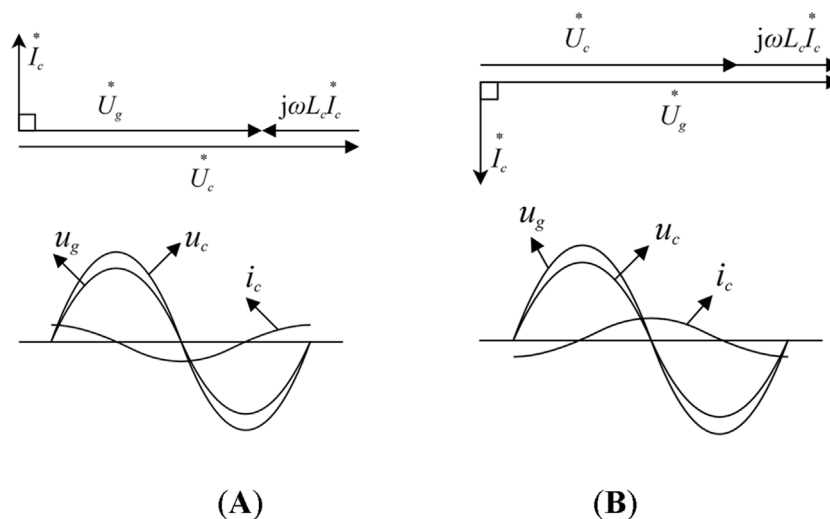


FIGURE 2 Phasor Diagram of STATCOM Operation, where (A) indicate the capacitive operating condition and (B) indicate the inductive operating condition.

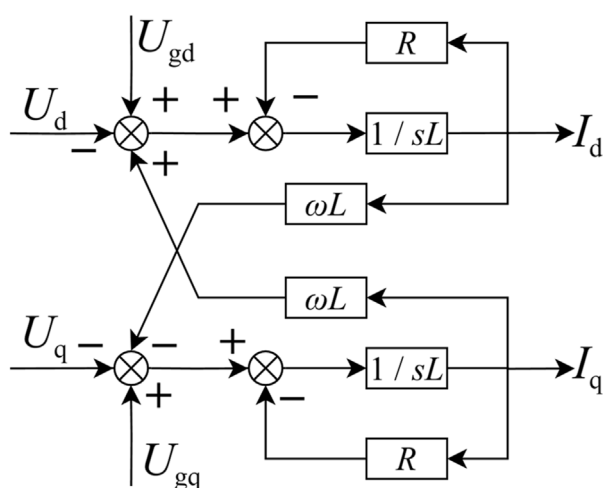


FIGURE 3 Block diagram of STATCOM plant in the dq reference frame.

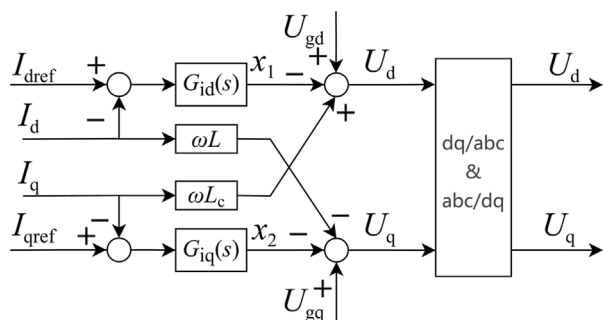


FIGURE 4 Controller structure of STATCOM in the dq reference frame.

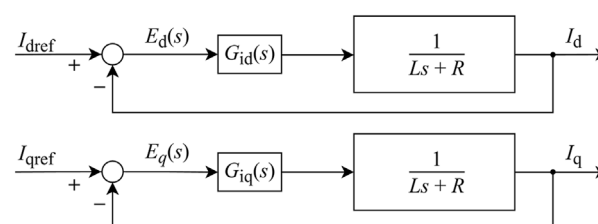
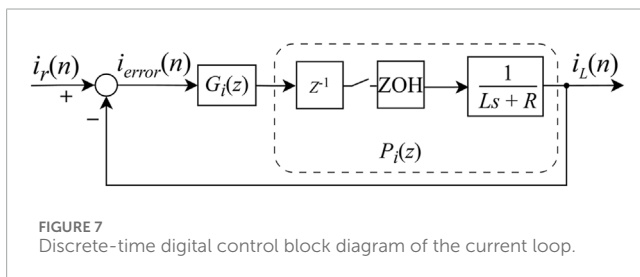
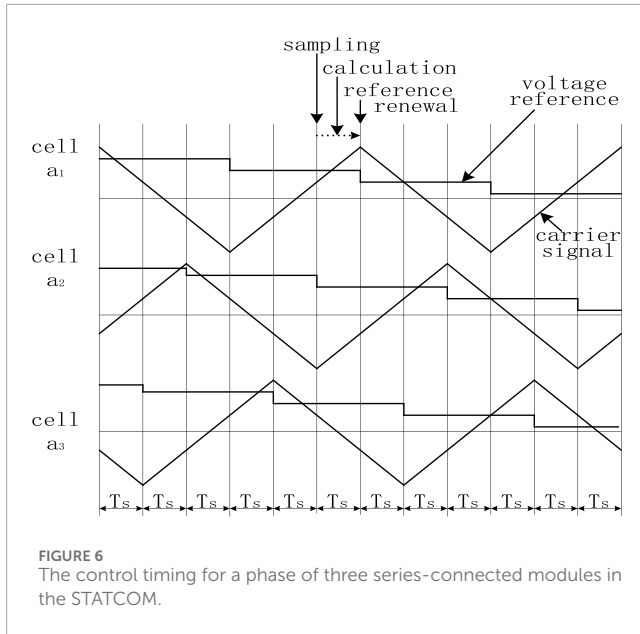


FIGURE 5 Equivalent control structure for active and reactive current loops.

the two arms share identical triangular carrier signals, while their reference signals are inverted. Across the cascaded H-bridge units, the triangular carriers are uniformly distributed over a 180° phase shift. Harmonic analysis of the unipolar double-frequency converter indicates that the equivalent output switching frequency using CPS-PWM reaches $2N$ times the carrier frequency (Akagi et al., 2017b; Wu, 2006), where N is the number of cascaded H-bridge modules. Under low switching frequency operation, the combination of module cascading and unipolar CPS-PWM not only increases the effective switching frequency—thus reducing switching losses—but also significantly improves the output voltage waveform quality by lowering total harmonic distortion (THD) (Basnet and Roinila, 2024b). This topology and modulation scheme is particularly well suited for high-power applications.

In the digital control system implementation, each H-bridge module updates its PWM reference signal at both the peak and valley points of the triangular carrier waveform. As a result, each phase effectively updates the reference signal $2N$ times within one carrier period, aligning the control frequency with the system's equivalent switching frequency. Considering inherent delays in the digital control process—such as sampling, data holding, and computational latency—a one-step delayed update scheme is adopted for the PWM



reference output. Accordingly, the control sampling period is set to one $2N$ -th of the carrier cycle. Depicted in Figure 6 is the control timing for a phase of N series-connected modules in the STATCOM, where $N = 3$. Owing to calculation delays, the voltage reference update is invariably delayed by one sampling period, T_s . Control timing sequence for one phase of the STATCOM with three cascaded H-bridge modules, illustrating the sampling instant, computation delay, zero-order hold, and PWM update process. The diagram clarifies how the discrete-time controller synchronizes with the carrier-based CPS-PWM strategy.

The discrete-time digital control block diagram of the STATCOM current loop is shown in Figure 7, where $G_i(z)$ represents the digital current regulator, z^{-1} denotes the one-sample delay in the control output, ZOH stands for the Zero-Order Hold, and the physical plant consists of the filter inductance L and equivalent resistance R .

The transfer function of ZOH in the s -domain is shown in Equation 6:

$$G_h(s) = \frac{1 - e^{-Ts}}{s} \quad (6)$$

The ZOH, combined with the filter inductance L and resistance R , constitutes a continuous-time low-pass subsystem. After discretization, and together with the one-sample delay element z^{-1} , they form the generalized plant $P_i(z)$ of the digital current control loop. Its Z-domain (discrete-time frequency domain) expression

is given as follows (Franklin et al., 2006), where $Z[\cdot]$ denotes the Z-transform of the continuous-time components inside the brackets. Here, ZOH denotes the zero-order hold operator, and z^{-1} represents the inherent one-sample delay introduced by digital control implementation.

$$P_i(z) = z^{-1} \cdot Z \left[\frac{1 - e^{-Ts}}{s} \cdot \frac{1}{sL + R} \right] = \frac{1 - e^{-\frac{R}{L}T}}{R} \cdot \frac{z^{-2}}{1 - e^{-\frac{R}{L}T}z^{-1}} \quad (7)$$

The open-loop current path consists of the current regulator $G_i(z)$ and the generalized plant $P_i(z)$, yielding the following closed-loop transfer function in the Z-domain:

$$\phi_i(z) = \frac{G_i(z)P_i(z)}{1 + G_i(z)P_i(z)} \quad (8)$$

If the desired Z-domain closed-loop transfer function is specified, the controller expression $G_i(z)$ can be derived accordingly based on Equation 8:

$$G_i(z) = \frac{1}{P_i(z)} \cdot \frac{\phi_i(z)}{1 - \phi_i(z)} \quad (9)$$

The requirement of deadbeat control is that the closed-loop system reaches a steady state with zero error in the minimum number of sampling periods for a given input, which inherently imposes constraints on the system's Z-domain transfer function.

Based on Equation 8, the Z-domain transfer function of the current loop error can be derived as follows:

$$\phi_{i_{error}} = \frac{1}{1 + G_i(z)P_i(z)} \quad (10)$$

In Figure 7, the reference input of the current control loop $i_r(n)$ is derived from the active and reactive current commands via Equation 5. During a reactive power change, the current reference is typically considered a step signal, whose Z-transform is calculated in Equation 11:

$$I_r(z) = \frac{1}{1 - z^{-1}} \quad (11)$$

Combining with

appear in the closed-loop transfer function. Specifically, the closed-loop transfer function $\phi_i(z)$ must include the plant's inherent delay term z^{-1} . Furthermore, the orders of $\phi_{i_error}(z)$ and $\phi_i(z)$ must be equal. The general form of these transfer functions with undetermined coefficients can be expressed as:

$$\begin{cases} \phi_{i_error}(z) = (1 - z^{-1})(1 + f_{11}z^{-1}) \\ \phi_i(z) = z^{-1}(f_{21}z^{-1}) \end{cases} \quad (14)$$

Subject to the following constraint:

$$\phi_{i_error}(z) = 1 - \phi_i(z) \quad (15)$$

Solving Equations 14, 15, yields: $f_{11} = f_{21} = 1$. Thus, the discrete-time closed-loop current transfer function and current error transfer function are shown in Equation 16:

$$\begin{cases} \phi_i(z) = z^{-2} \\ \phi_{i_error}(z) = 1 - z^{-2} \end{cases} \quad (16)$$

From the expression of $\phi_i(z)$, it is evident that the two poles of the discrete closed-loop system are both located at the origin, corresponding to a two-sample delay in input tracking with zero steady-state error.

Furthermore, based on Equations 7, 9, the Z-domain expression $G_i(z)$ of the deadbeat current controller can be derived as:

$$G_i(z) = \frac{R}{1 - e^{-\frac{R}{L}T}} \cdot \frac{1 - e^{-\frac{R}{L}T}z^{-1}}{1 - z^{-2}} \quad (17)$$

Equation 17 defines the final form of the deadbeat current regulator, whose structure inherently includes predictive and derivative characteristics, providing superior transient response. Discretizing a PID transfer function via the Tustin method yields the following z-domain form:

$$G_i(z) = \frac{(k_p + k_i \frac{T}{2} + k_d \frac{2}{T}) + (k_i T - k_d \frac{4}{T})z^{-1} + (-k_p + k_i \frac{T}{2} + k_d \frac{2}{T})z^{-2}}{1 - z^{-2}} \quad (18)$$

Where k_p , k_i , and k_d represent the proportional, integral, and derivative gains of the PID controller, respectively. Equations 17, 18, are mathematically equivalent in structure, but differ in the method of obtaining coefficients. Since its mathematical structure is similar to that of PID, the implementation of a deadbeat controller is very straightforward. Like PI controllers, PID controller parameters typically require selection based on empirical bandwidth estimation and iterative tuning (Shen, 2021).

From another perspective, the deadbeat controller proposed in this paper can be regarded as a PID controller whose parameters are derived analytically rather than through heuristic tuning (Mattavelli, 2005). Due to the inclusion of a derivative term, the controller theoretically provides faster dynamic response than a PI controller (Elhassan et al., 2022). Moreover, the design process does not rely on analog-domain knowledge or experience, offering a fully digital approach to controller design.

4 Simulation and stability analysis

To verify the proposed method, a simulation model of the CHB-STATCOM was built in Matlab Simulink. Key parameters are shown in Table 1:

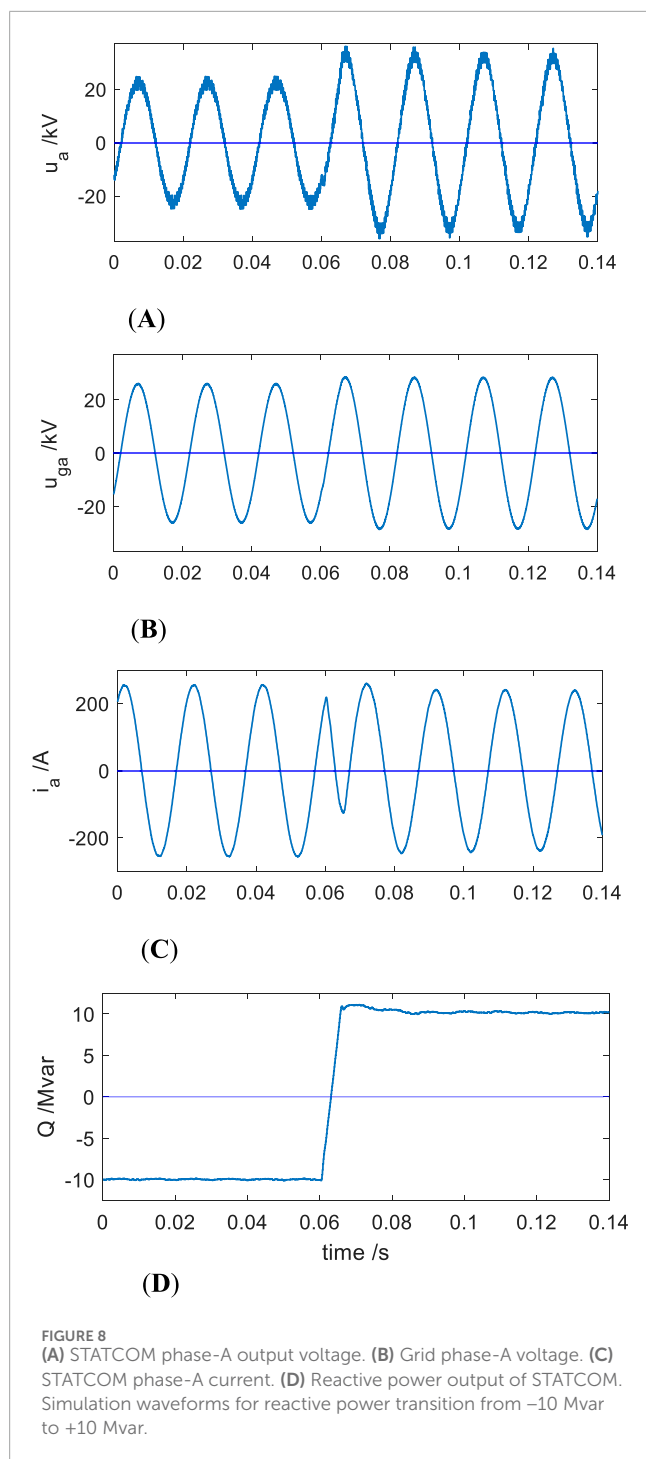
TABLE 1 Parameters of the STATCOM simulation model.

Parameter name	Value
Grid Frequency	50 Hz
Rated Capacity	12 Mvar
Rated Voltage	35 kV
Filter Inductance	37.9 mH
Equivalent Resistance	238 mΩ
Modules per Phase	20
Switching Frequency	200 Hz
DC Voltage per Module	1750 V
Capacitance per Module	2 mF
Grid Impedance	$2 + j200 \text{ m}\Omega$

Based on the model parameters, the equivalent switching frequency of the digital controller is calculated as $2 \times 20 \times 200 = 8 \text{ kHz}$, corresponding to a sampling control period of $125 \mu\text{s}$. According to Equation 17, the resulting controller transfer function is: $\frac{303.3 - 303.1z^{-1}}{1 - z^{-2}}$.

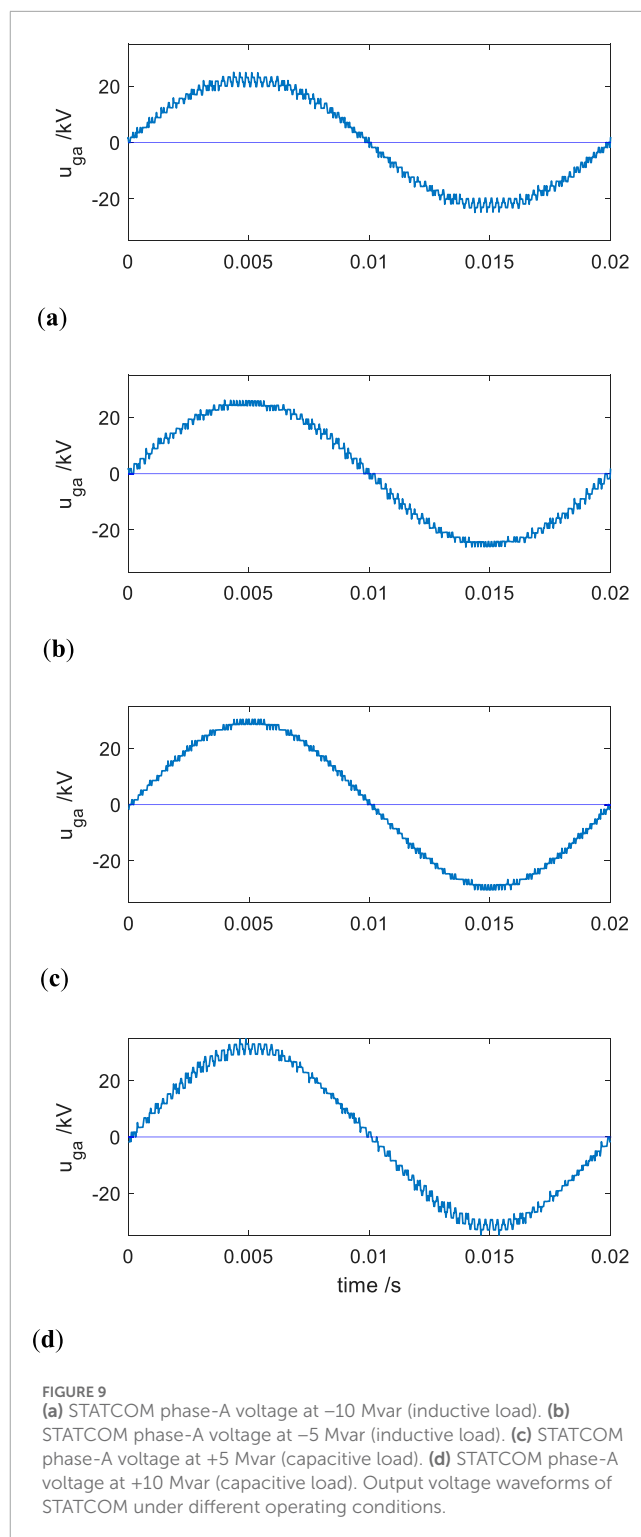
Figure 8 shows the simulation waveforms. The initial reactive power reference is set to -10 Mvar , and at 0.6 s , it switches to $+10 \text{ Mvar}$. A positive reference corresponds to inductive reactive power, while a negative reference indicates capacitive operation.

Figure 8A illustrates the multilevel output voltage waveform of phase A from the STATCOM, and Figure 8B shows the corresponding grid voltage waveform of phase A. The STATCOM output voltage remains in phase with the grid voltage throughout the process. In inductive operation, the STAT



greater number of voltage levels. Under a PWM carrier frequency of 200 Hz, the proposed dq-based deadbeat current control method enables the generation of highly sinusoidal multilevel output waveforms (Basnet and Roinila, 2024b).

Table 2 compares the total harmonic distortion (THD) of output current between the proposed deadbeat control method and a conventional proportional-integral (PI) controller. The comparison clearly shows that the deadbeat method provides superior current waveform quality. This is consistent with earlier analytical results: although the deadbeat digital controller is

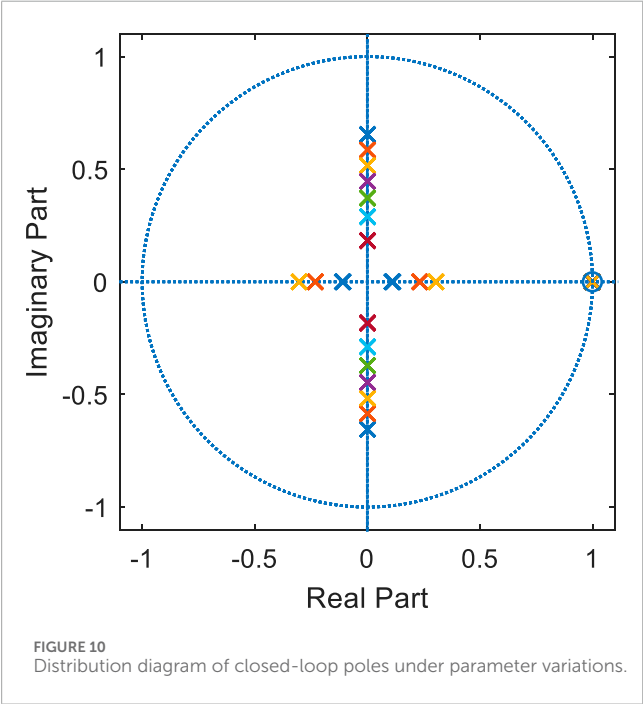


functionally similar to a continuous-time Proportional-Integral-Derivative (PID) controller, its parameter design method is fundamentally different. The deadbeat controller parameters are directly calculated from Equation 17, eliminating the need for iterative tuning.

In contrast, conventional PI controllers lack a derivative component and must rely on increasing the proportional gain

TABLE 2 Comparison of output current THD: PI control vs deadbeat control.

Type of control method	Full capacitive load	Half capacitive load	Full inductive load	Half inductive load
PI control	0.58%	1.28%	1.42%	0.77%
Deadbeat control	0.56%	0.98%	1.14%	0.63%



to improve response speed. However, excessive gain can lead to instability. Implementing a classical PID controller would require a more complex tuning process, often involving multiple iterations, making it difficult to achieve optimal performance in a single design cycle.

The THD values for all tested load conditions are consistently lower under deadbeat control, verifying the method’s capability to maintain waveform quality even during load transitions. The deadbeat control method exhibits excellent fast-response characteristics. However, in a closed-loop control system, speed and stability are often inherently contradictory objectives. During simulation analysis, the inductance and resistance parameters are assumed to be fixed. In practical scenarios, however, deviations in component values are inevitable. It is assumed that the STATCOM’s filter inductance may vary by $\pm 10\%$ from its nominal value, and the equivalent resistance may vary within the range of -10% to $+40\%$. The parameter tolerance ranges of $\pm 10\%$ for inductance and -10% to $+40\%$ for resistance are chosen to reflect typical manufacturing deviations and operating temperature variations encountered in utility-scale STATCOM hardware.

Based on these tolerance ranges for L and R, the boundary conditions of the plant parameters are defined, and the pole distribution of the closed-loop system under deadbeat current control is plotted, as shown in Figure 10.

As observed from Figure 10, the closed-loop system contains a pair of complex conjugate poles and one real pole, all located within the unit circle, indicating that the system remains stable. The real pole lies close to a real-axis zero, forming a pole-zero pair that essentially cancels out and thus has a negligible influence on the dynamics of the current loop. Consequently, the complex conjugate poles become the dominant factor affecting system performance. Although the poles shift outward under parameter variations, the root locus remains within the unit circle, indicating system stability and robustness to component tolerances (Li et al., 2020).

As actual parameters deviate from their nominal design values, the complex conjugate poles gradually move outward from the origin along the left side of the imaginary axis. Simulation results confirm that satisfactory current waveform quality is maintained across the full range of parameter variations.

5 Discussion

The simulation results presented in this study demonstrate that the proposed dq-based deadbeat current control method achieves rapid dynamic response and zero steady-state error under various operating conditions. Compared with conventional PI controllers, which often require iterative tuning and are sensitive to parameter variations, the deadbeat controller exhibits consistent performance across a wide range of system configurations and component tolerances. This robustness is particularly valuable in high-voltage multilevel STATCOM systems, where parameter mismatches and switching frequency constraints are common.

The success of the deadbeat strategy stems from two core features: the direct design in the discrete-time domain and the transformation of sinusoidal current references into DC quantities via the dq coordinate system. These features simplify the control problem, allowing for exact, closed-form computation of control voltage inputs. Unlike existing deadbeat methods applied in stationary reference frames—which are limited by their inability to fully eliminate steady-state error—the proposed dq-domain approach enables accurate and stable tracking without sacrificing control responsiveness.

From a systems integration perspective, the method also supports low switching frequencies, which is advantageous for reducing switching losses and improving the efficiency of cascaded H-bridge (CHB) STATCOMs. The observed total harmonic distortion (THD) results confirm that the proposed method generates high-quality current waveforms, even under dynamic reactive power transitions. This aligns with findings in recent studies that advocate for control strategies tailored directly in the digital domain (Carrasco et al., 2006) to overcome discretization-induced limitations in classical controllers. During practical

implementation, the sampling interval must meet the requirements for computational real-time performance. Additionally, signal filtering is also a critical aspect. The bandwidth of the current filter should be set as close as possible to half of the sampling frequency in order to achieve the desired rapid control response.

However, certain practical challenges remain. The controller assumes ideal capacitor voltage balance across all H-bridge modules, which may not hold in real-world implementations. Unequal DC capacitance or charge accumulation can introduce voltage imbalance that may interfere with the current control loop. Further research is needed to investigate how local voltage balancing strategies interact with the global current regulation scheme (Cheng et al., 2024; Jin et al., 2018). Additionally, parameter optimization for more complex grid disturbances (Arya and Singh, 2013), non-ideal measurement feedback, and communication delays represent important directions for future work. Exploring adaptive or learning-based extensions of the deadbeat framework could also enhance its applicability in evolving power grid environments (Yang et al., 2024).

6 Conclusion

This paper presents a discrete-time deadbeat current control method for STATCOM systems based on the dq reference frame. By designing the controller directly in the digital domain and using coordinate transformation to simplify current regulation, the proposed approach achieves fast, accurate, and robust performance without requiring iterative parameter tuning. Simulation results validate its effectiveness under diverse operating conditions, confirming its potential as a practical and high-performance solution for modern STATCOM applications.

Data availability statement

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation.

Author contributions

HL: Conceptualization, Methodology, Project administration, Writing – original draft. AM: Conceptualization, Methodology, Writing – original draft. YaZ: Conceptualization, Writing – review

and editing. YiZ: Writing – review and editing, Formal Analysis. SZ: Writing – original draft, Writing – review and editing. YuZ: Writing – review and editing, Project administration. YwZ: Writing – review and editing, Resources. ZT: Funding acquisition, Writing – review and editing.

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Conflict of interest

Authors HL, YaZ, YiZ, SZ, YuZ, YwZ, and ZT were employed by Inner Mongolia Wuhai Ultra High Voltage Power Supply Bureau. Author AM was employed by Inner Mongolia Electric Power Research Institute.

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