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EDITED BY
Anshu Kumari,
Physical Research Laboratory, India

REVIEWED BY
Harsha Avinash Tanti,
Indian Institute of Technology Indore, India
Vaibhav Rathore,
Physical Research Laboratory, India

*CORRESPONDENCE
Jianing Rao,
raojianing@nssc.ac.cn

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A novel space intelligent computing and data processing architecture--the spacecraft payload health management unit (SPHMU)

Wenjie Zhao[1,2], Jianing Rao[1,2]*, Miao Ma[1], Jianzhe Zhang[1], Shuanglong Li[1], Wenyuan Jia[1], Zhenxing Dong[1,2], Baocheng Hou[1], Guofeng Xue[1], Guodong Yin[1,2], Yan Zhu[1,2] and Junshe An[1,2]

[1]National Space Science Center, The Chinese Academy of Sciences, Beijing, China, [2]University of Chinese Academy of Sciences, Beijing, China

This paper primarily introduces a novel on-board intelligent computing and intelligent data processing architecture. This architecture leverages the collaborative work of high reliability computers (HRC) and high performance computers (HPC) to achieve highly reliable payload management and data interaction, as well as high-performance intelligent computing and data processing objectives in space application environments. This paper implements the novel on-board intelligent computing and intelligent data processing architecture using a combination of HRC and HPC. Specifically, HRC is responsible for data interaction with the spacecraft bus, including telemetry, telecommand, and control (TT&C) information of various payloads, as well as time and space information. HPC, on the other hand, primarily executes application software (APP) to process the received payload data. This includes computationally intensive tasks such as attitude and orbit determination. Communication between HRC and HPC is facilitated through a high reliability field programmable gate array (FPGA). This paper verifies the stability of this architecture through rigorous testing at the aerospace level. The novel on-board intelligent computing and intelligent data processing architecture possesses excellent computing capabilities, spatial adaptability, reliability, and a flexible structure, laying a foundation for high-performance computing in space.

KEYWORDS

intelligent computing, intelligent data processing, attitude and orbit, high-reliability computer, high-performance computer

1 Introduction

The rapid advancement of China's aerospace technology has driven the increasing prioritization of on-board computational capabilities and data processing efficiency across diverse space missions. These missions, spanning from space station operations to near-Earth surveillance, medium/high-orbital exploration, and deep-space investigations, now mandate stringent requirements for equipment miniaturization, weight reduction, and power consumption optimization.

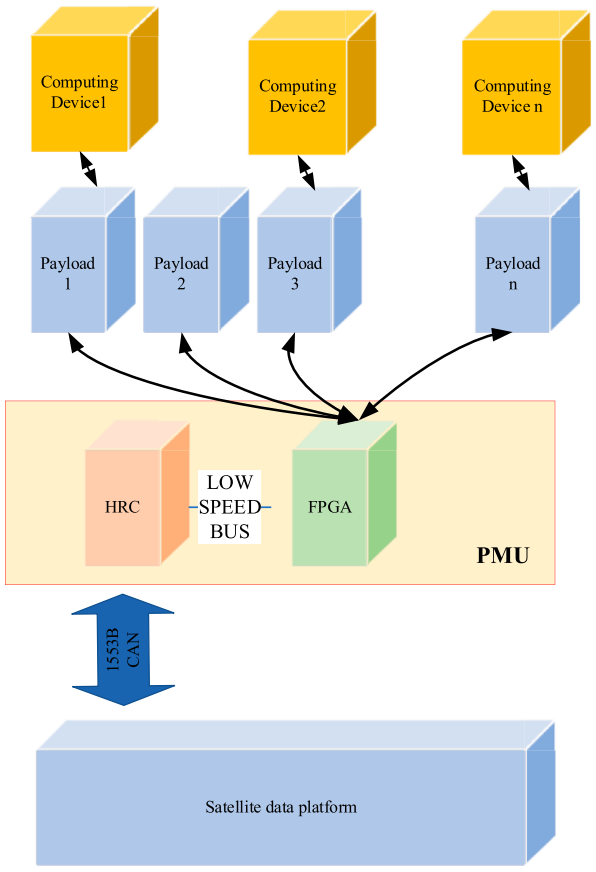

FIGURE 1
Traditional payload management unit.

Consequently, highly integrated intelligent load management systems are becoming critical components in modern aerospace platforms. Such devices exhibit compact physical dimensions, ultra-lightweight construction, multi-core heterogeneous computing architectures, and radiation-hardened reliability characteristics essential for next-generation mission-critical applications.

A Payload Management Unit (PMU) serves as a critical component in various systems, ensuring the effective operation and integration of payloads. These systems range from spacecraft and satellites to unmanned aerial vehicles (UAVs) and industrial equipment. The PMU's functions include power distribution, data handling, thermal management, and communication interface, all tailored to the specific requirements of the payload and the overall system (Del Castillo et al., 2025; Zhou and An, 2013).

In spacecraft, a PMU is essential for managing the power, data, and control signals between the spacecraft and its scientific instruments or other payloads. These systems highlight the importance of efficient payload management in enhancing mission readiness and mitigating risks (Del Castillo et al., 2025). Traditional PMUs inherently lack high-performance computational capabilities, as illustrated in Figure 1, necessitating continuous advancements in on-board high-performance computing (OHPC) to meet the evolving demands of space missions.

TABLE 1 The dimensional and mass characteristics of the SPHMU.

Parameter	Value
Maximum size (mm)	295 ± 2 × 130 ± 2 × 189 ± 2
Body size (mm)	249 ± 2 × 118 ± 2 × 178 ± 2
Installation dimensions (mm)	259 ± 2 × 118 ± 2
Total mass (kg)	6.0 ± 0.5

In response to these evolving requirements, we have designed a highly innovative Space Payload Health Management Unit (SPHMU) for a specific spacecraft program, realizing a high-integration, high-reliability device for spaceborne intelligent computing and intelligent data processing. Compared to traditional payload management units, this SPHMU retains a High-Reliability Computer (HRC) while integrating a High-Performance Computer (HPC) dedicated to high-performance space computing and data processing; thus, it not only maintains the fundamental payload management and data processing functions of traditional units but also provides significantly enhanced computational capabilities for tasks such as attitude and orbital determination, orbital maneuver calculation, and autonomous operations, establishing a robust high-performance software and hardware platform that offers excellent adaptability and scalability for supporting diverse scientific mission objectives (Abdu et al., 2023; Ramírez et al., 2022; Ben Yahia et al., 2025). The dimensional and mass characteristics of the SPHMU are presented in Table 1.

As illustrated in Figure 1, the traditional payload management unit solely facilitates high-speed data transmission and data processing between various payloads, as well as high-speed data transfer and telemetry and telecommand (TT&C) operations with the Satellite data platform; however, this necessitates distributing the data returned from the spacecraft bus back to individual payloads, leading to distributed computations and data processing among the payloads themselves which impose significant resource overhead in terms of weight and power consumption, while simultaneously the transmission of this data substantially consumes bus bandwidth resources (Bhandari et al., 2024).

The operational architecture of the SPHMU (Space Payload Health Management Unit) designed for a specific mission model is shown in Figure 2, embodying a highly integrated and reliable platform for spaceborne intelligent computing and intelligent data processing. Compared to traditional payload management units, this SPHMU retains a High-Reliability Computer (HRC) while integrating a High-Performance Computer (HPC) dedicated to spaceborne high-performance computing and data processing. Consequently, it not only maintains fundamental payload management and data processing capabilities inherent to conventional units but also delivers advanced computational functionalities, including real-time precision orbit determination software, autonomous orbital maneuver software for elliptical trajectories, and intelligent on-orbit data analysis with anomaly alert systems. These functionalities are deployed as software applications (Apps) via a software-defined hardware platform,

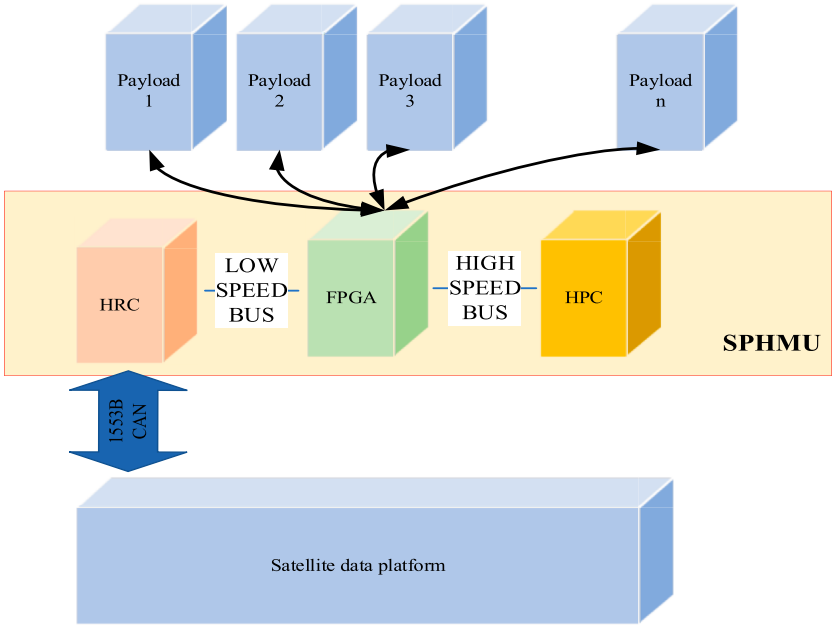

FIGURE 2
SPHMU work mode.

enhancing operational flexibility and mission adaptability (Hui et al., 2025; Morton et al., 2021).

2 System design of SPHMU

2.1 Overall hardware design

In order to adapt to different data interfaces with different loads, the designed SPHMU hardware includes RS422 data interfaces, LVDS data interfaces, AD data acquisition interfaces, OC output data interfaces, Ethernet interfaces, USB interfaces, 1553B bus interfaces, CAN bus interfaces, Mass storage interfaces and program data storage interfaces. These interfaces can connect with actual payload electronics and the satellite data platform, providing sufficient data processing capabilities and a sufficient number of data interfaces, making it practically applicable to various payload electronics through different configurations.

The SPHMU comprises five integrated components as illustrated in Figure 3: a Power Supply Unit, an HRC (High-Reliability Computer) Unit, an HPI (High-Performance Interface) Unit, and two HPC (High-Performance Computer) Units (HPC-A and HPC-B). The Power Supply Unit converts bus power into secondary power outputs (e.g., 5V, 3.3V) required by the system (Martins et al., 2024).

The HRC Unit, responsible for external data interfaces, data storage, and control functions, collects payload status from the HPI Unit and exchanges data with the spacecraft management system via a configurable MIL-STD-1553B or CAN bus. It further monitors and manages the current, voltage, and operational status of the HPC Units. Architecturally, the HRC integrates a radiation-hardened CPU, SDRAM, NOR Flash, a watchdog timer, a refresh controller, transformers, and MIL-STD-1553B transceivers. Its

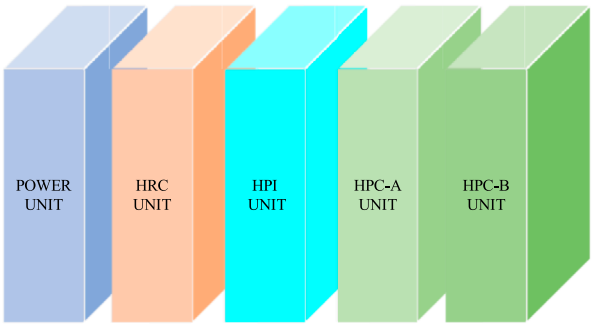

FIGURE 3
The SPHMU design block diagram.

core employs the Loongson XX300 processor from Loongson Technology, designed for space applications with a total ionizing dose (TID) tolerance ≥300 krad(Si) and a single-event latch-up (SEL) threshold ≥75 MeV·cm^2/mg. To mitigate single-event upsets (SEUs), the CPU implements error-correcting code (ECC) for SDRAM; additionally, it supports dual program memory sectors for booting—selectively activated during power-on reset or watchdog reset—thus avoiding system failure due to corruption in a single memory sector and enhancing overall reliability.

The High-Performance Interface (HPI) Unit primarily facilitates external communication via RS422 interfaces, LVDS interfaces, analog signal acquisition, switch command (OC) control, and memory management, utilizing a hardware architecture comprising an FPGA, analog multiplexers, amplifiers, ADCs, OC circuits, and

NAND Flash. Specifically, the FPGA—implemented using a SRAM-based device from Xilinx—operates as a critical bridge between the HRC and HPC units: it exchanges scientific data with the HPC units via a high-speed internal bus while simultaneously transmitting status information to the HRC unit through a low-speed internal bus, thus serving as the core interconnect mechanism for bidirectional data and control pathways (Zhao et al., 2022).

The High-Performance Computing (HPC) Unit primarily comprises a high-performance CPU, peripheral memory modules, and interface circuitry, collectively enabling the bootloading of the Linux operating system, execution of user-installed applications, and processing of diverse data transmitted from the High-Reliability Monitoring Module, as well as performing critical functions such as precision orbit determination, elliptical orbit maneuver calculations, and intelligent data analysis with anomaly alerting. Designed as a standardized board-level solution, this unit integrates a Loongson XX2000 CPU (manufactured by Loongson Technology), DDR4 SDRAM, SPI Flash, eMMC storage, watchdog circuitry, Ethernet ports, USB interfaces, HDMI output, DC/DC converters, and debugging circuits. The XX2000 CPU—fabricated using a 28 nm FD-SOI process and meeting industrial-grade (IND) quality standards—exhibits a total ionizing dose (TID) tolerance exceeding 100 krad(Si) and complete immunity to single-event latch-up (SEL). Architecturally, the CPU incorporates dual LA364 cores operating at 0.8–1.2 GHz, a 72-bit DDR3/4 memory controller, and comprehensive system peripheral I/Os, thereby consolidating computational robustness with radiation-hardened reliability for spaceborne applications.

2.2 1553B&CAN bus design

The SPHMU employs a configurable dual-bus architecture integrating both MIL-STD-1553B and CAN bus standards as its critical communication backbone (Figures 4, 5), with meticulous design considerations paramount due to their fundamental role in mediating payload status monitoring and spacecraft command execution; specifically, this architecture implements cold redundancy with duplicated A/B channels for both bus types, significantly enhancing system fault tolerance through hardware-based redundancy while strictly adhering to spacecraft bus design specifications, thereby ensuring robust signal integrity through controlled impedance routing, electromagnetic interference (EMI) shielding, and validated signal termination protocols across all mission operating conditions.

RS422 and LVDS are both signal transmission technologies widely used in industrial, communication, and embedded systems, characterized by their high efficiency, stability, and strong anti-interference capabilities.

Taking the 1553B bus as an example, each word (command word/data word/status word) is fixed at 20 bits (3 synchronization heads+16 data bits+1 odd parity bit), with a transmission rate of 1 Mbps. The transmission time of a single word is Equation 1:

$$T_{word} = \frac{20}{1Mbps} = 20\,\mu s \tag{1}$$

Considering the message interval (standard requirement ≤14 μs) and protocol overhead (command word, status word), the actual effective bandwidth is significantly reduced. For example, the actual efficiency of transmitting 32 data words is approximately (Equation 2):

$$\eta_{actual} = \frac{32 \times 16}{(34 \times 20) + 14} \approx 68\% \tag{2}$$

To reduce reflection and noise, the terminal resistance needs to match the cable characteristic impedance (usually 78 Ω) and be verified by the following Equation 3:

$$Z_{match} = \frac{Z_{cable}}{2} \tag{3}$$

The characteristic impedance of twisted pair cable is about 78 Ω.When indirectly coupled, the terminal resistor is directly integrated onto the coupler.

Taking CAN bus as an example, the explicit level requirement is Equation 4:

$$V_{diff\_dom} = V_{CAN\_H} - V_{CAN_L} \geq 1.5V \tag{4}$$

Implicit level requirement (Equation 5):

$$V_{diff\_dom} = V_{CAN\_H} - V_{CAN_L} \geq 0.5V \tag{5}$$

Common mode voltage tolerance (Equation 6):

$$-2V \leq V_{CM} \leq 7V \tag{6}$$

Terminal resistors need to be deployed at both ends of the bus to suppress signal reflection (Equation 7):

$$R_{term} = \frac{Z_0}{2} = 120\Omega \pm 5\% \tag{7}$$

The formula for signal quality assessment is (Equation 8):

$$S_{total} = \frac{W_{edge} \times S_{edge} + W_{amp} \times S_{amp} + W_{ref} \times S_{ref}}{W_{total}} \tag{8}$$

Typical settings (W_{edge}, W_{amp}, W_{ref}) = (50%, 25%, 25%)

S_{edge} scores the edge rate (0%–100%), and scores 100% when the edge time t_{edge} is less than 10% and the bit time is less than 10%

S_{amp} is a stable amplitude rating.

S_{amp} = 100%. When $U_{distortion}$ = V_{diff_dom} ≥2.2V, $U_{disturb}$ is the minimum difference between explicit/implicit levels.

S_{ref}: Reflection Distortion Score. S_{ref} = 100% when U_{pp} = $U_{disturb}$ (no overshoot/undershoot).

The transmission speed of CAN bus is relatively high, so twisted pair cables are used in PCB design, with a line length matching error of ≤5 mil to avoid branching (stub length <3 cm).

2.3 HPC hardware design

The HPC unit employs Loongson Zhongke's XX2000 processor chip, interfacing with a 32 GB eMMC module via the eMMC interface to store the operating system and application data, where the eMMC chip is specifically selected for single-event latch-up (SEL) immunity to mitigate radiation-induced failures in space environments. To enhance system reliability, triple-redundant kernel images are stored in partitioned sectors

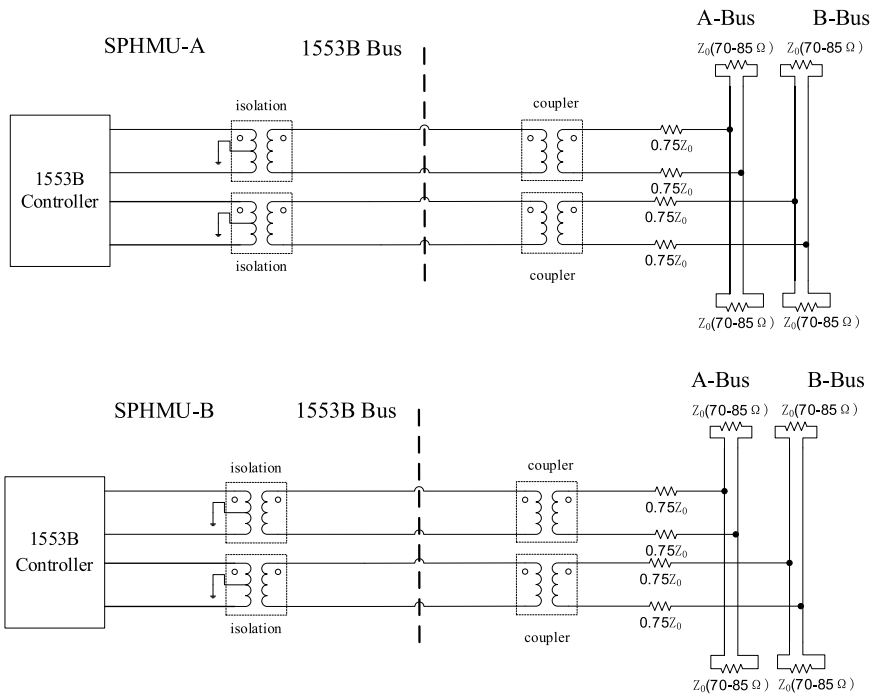

FIGURE 4
The complex 1553B Bus construction standards.

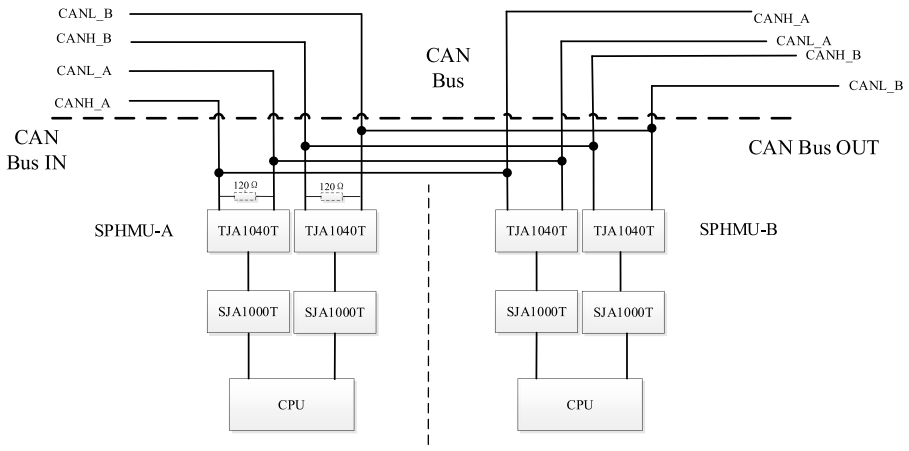

FIGURE 5
The complex CAN Bus construction standards.

of the eMMC, and during boot initialization, a two-out-of-three voting mechanism is executed to validate kernel integrity, thereby preventing boot failures caused by anomalies in any single storage region. The SPI Flash is dedicated to hosting the CPU's bootloader firmware, while the eMMC exclusively maintains the full operating system and application binaries.

For computational operations, the HPC unit receives multi-channel telemetry data through inter-layer connectors from the HPI unit for on-orbit real-time processing, concurrently feeding its own operational telemetry back to the high-reliability monitoring unit. Comprehensive debugging and expansion interfaces—including serial port (UART), USB, Gigabit Ethernet, and HDMI—are integrated into the high-performance CPU to facilitate hardware/software diagnostics and peripheral connectivity.

2.4 Space reliability design of SPHMU

As illustrated in Figure 2, scientific data from external payloads are transmitted via multiple bus interfaces to the FPGA within

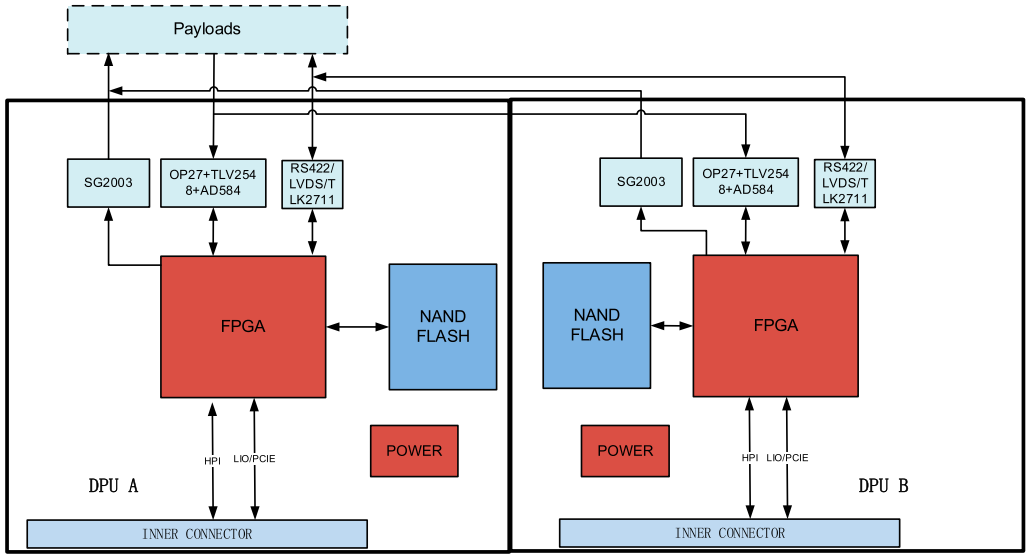

FIGURE 6
The DPU of SPHMU.

the SPHMU for on board storage and preliminary processing. The integrated data processing unit employs a dual-layer redundancy architecture comprising primary redundancy and cross-redundancy mechanisms to ensure operational reliability in space environments.

As shown in Figure 6, the design block diagram of the data processing unit (DPU) for SPHMU is presented. Due to the connection of different payloads, redundant system backup design and hardware interface cross-backup design are implemented. Radiation-hardened high-reliability components are selected to avoid single-point failures, thereby ensuring equipment reliability.

The external data bus of the data processing unit integrates LVDS, RS422, and 2,711 bus architectures, achieving a maximum operational bandwidth of 2.4 Gb/s. The internal bus system comprises HPI (HRC), PCIe 2.0 (HPC), and LIO (HPC) interconnects—three CPU-native communication protocols with peak data transfer rates up to 1 GB/s. FPGA and HPC achieve slow and fast data interaction through the CPU's built-in LIO bus (1 Mbps) and PCIe bus (1 GB/s) respectively, as shown in Figure 7.

For space environmental reliability, the majority of components employ radiation-hardened devices with a total ionizing dose (TID) tolerance ≥300 krad(Si) and single-event latch-up (SEL) threshold ≥75 MeV·cm^2/mg. For components not meeting single-event effect (SEE) requirements, mitigation measures including tantalum shielding implementation, ECC-based software redundancy, and FPGA periodic refresh mechanisms are integrated. Additionally, a homogeneous primary/backup architecture is adopted for critical systems, with redundant interfaces employing dual-channel failover protocols to ensure operational continuity under extreme space radiation conditions.

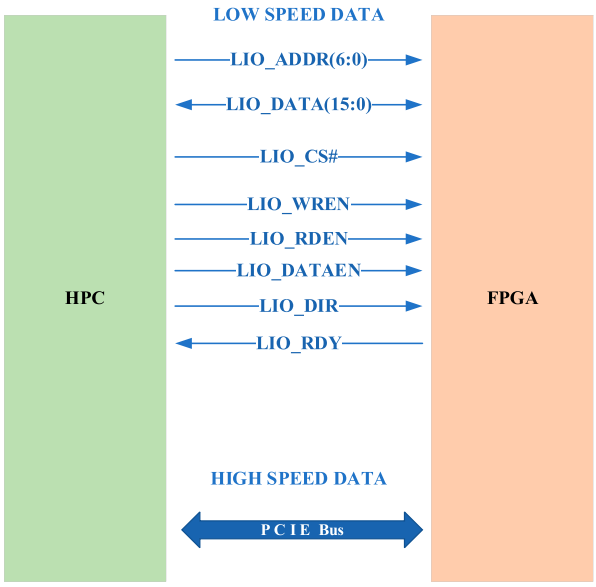

FIGURE 7
Data transmisson aarchitecture of FPGA and HPC.

2.5 Functional description of SPHMU

The SPHMU module supports a comprehensive set of interface standards with specific directionality and quantity configurations as enumerated in Table 2, including LVDS (Low-Voltage Differential Signaling), RS422 (differential serial communication), 1553B (MIL-STD-1553 avionics bus), CAN (Controller Area Network), OC, AD (Analog-to-Digital), mass storage interfaces, USB 3.0 (Universal Serial Bus 3.0), HDMI 2.1 (High-Definition Multimedia Interface 2.1), and Gigabit Ethernet.

TABLE 2 Interfaces Configuration by SPHMU.

Interface	I/O	Quantity
1553B	IN/OUT	4 channels
CAN	IN/OUT	4 Channels
RS422	IN	8 Channels
RS422	OUT	8 Channels
LVDS	IN	8 Channels
LVDS	OUT	8 Channels
OC	OUT	14 Channels
AD	IN	32 Channels
Mass Storge	IN/OUT	16 Tb
USB3.0	IN/OUT	6 Channels
Gigabit Ethernet	IN/OUT	2 Channels
HDMI2.1	IN/OUT	2 Channels
PCIE 2.0	IN/OUT	2 Channels

FIGURE 8
The UGT with SPHMU.

The test setup between the universal ground test (UGT) equipment and the SPHMU is shown in Figure 8.

3 Software design of SPHMU

In the previous section, We have proposed a detailed hardware design for the SPHMU. This design is compatible with most general interfaces, different construction standards, and communication protocols, and it provides an ample number of interfaces. This section primarily focuses on the software design of the SPHMU. Given the foundational nature of the software design implemented in both the HRC (High-Reliability Computer) unit and the HPI (High-Performance Interface) unit, this work concentrates its primary focus on detailing the software architecture and computational workflows deployed within the HPC (High-Performance Computing) unit, which encapsulates the system's advanced algorithmic processing, autonomous decision-making capabilities, and mission-specific application frameworks essential for next-generation spaceborne intelligence (Bhargav Reddy and Vijayreddy, 2025; Bhandari et al., 2024).

3.1 HRC unit software design

The HRC (High-Reliability Computer) unit management software is architecturally partitioned into four functional modules:

MIL-STD-1553B bus communication management, RS422 payload communication management, engineering telemetry management, and health monitoring with operational maintenance.

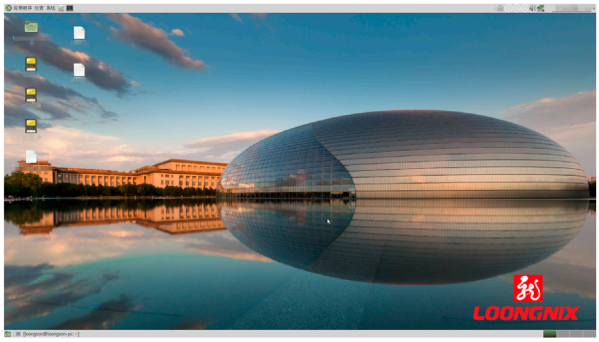

FIGURE 9
Linux program running interface of SPHMU.

TABLE 3 Conditions of thermal vacuum test.

Parameter	Acceptance level Requirements
Test pressure	≤6.65 × 10^{-3} Pa
Temperature eange	−25 ℃ to + 65 ℃
Cycle count	Primary Unit: 6 cycles Redundant Unit: 6.5 cycles
Temperature ramp rate	≥1 ℃/min

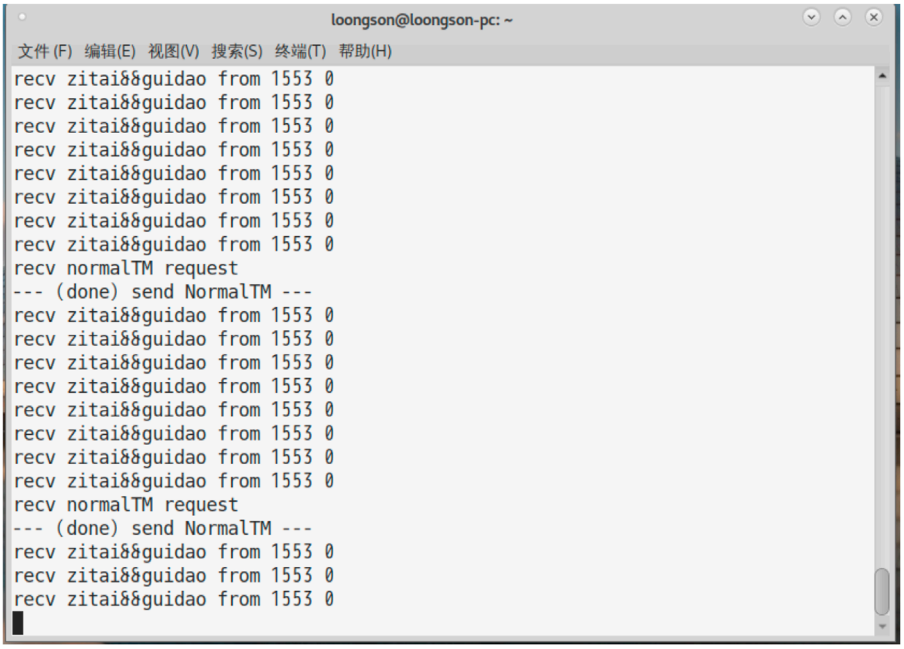

FIGURE 10
Operational execution of HPC Unit's sftware.

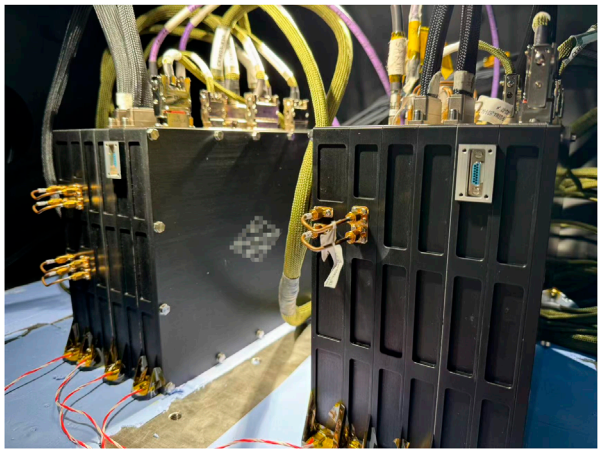

FIGURE 11
Sphmu in thermal vacuum test.

The 1553B communication module facilitates deterministic data exchange with the spacecraft management computer, encompassing reception of command directives and broadcast time-code messages alongside transmission of device engineering parameters.

Engineering telemetry management systematically aggregates operational status metrics from individual subsystems into consolidated telemetry parameters, periodically transmitting these datasets to the spacecraft management computer via the 1553B bus while concurrently packaging the Payload Health Manager's engineering parameters into standardized CCSDS-compliant telemetry source packets.

Health and maintenance operations integrate system preservation capabilities, encompassing initialization routines, time synchronization protocols, Error Detection and Correction (EDAC) processing, 1553B link integrity monitoring, and on-orbit software reconfiguration functionalities essential for sustained mission longevity.

3.2 HPC unit software design

Utilizing the Loongson-embedded operating system, the HPC unit delivers core functionalities including communication protocols for external devices and FPGA interfacing mechanisms, thereby establishing a robust foundation-layer infrastructure for upper-level application software.

The application support middleware orchestrates dynamic startup and termination of all software applications executing on the XX2000 processor, wherein it ingests inbound data packets and command instructions through standardized interfaces, executes protocol-compliant unpacking and parsing operations, and rigorously validates data integrity and command legality—automatically discarding invalid or noncompliant transmissions. Following command header interpretation, it autonomously executes locally managed directives while concurrently routing application-tier commands to designated targets. Beyond reception duties, the system aggregates internal state diagnostics and application runtime telemetry into unified CCSDS-compliant downlink packets.

Additionally, it administers essential maintenance operations encompassing system initialization, precision time synchronization, in-flight software updates, and cross-platform configuration

TABLE 4 Comparison results of OBCs (AAC Clyde Space, 2025).

Manufacturer/ Model	Processor architecture	Main frequency	Memory	Interface expansion	Application scenarios	Production countries
Xuanyu Space NANOSATPRO	SOC	200 MHz	4 MB Flash, 8 MB RAM	CAN、SpaceWire、1553B	Nanosatellites, CubeSats	China
Obit OBC	SPARC	100 MHz	16 MB Flash, 8 MB RAM	1553B、RS-232、LVDS	Military satellites, remote sensing satellites	China
LOONGSON XX2000	LoongArch	1.6 GHz	2 MB Cache 16 GB DDR4 SDRAM 16 Gb eMMC	PCIE、HDMI 、SATA、USB3.0、USB2.0 、CAN、PWM、LIO、eMMC、RGMII、DDR4	Low to medium orbit satellites, deep space exploration	China
AAC Clyde Space KRYTEN-M3	SPARC V8	50 MHz	8 MB Flash +4 MB SRAM	CAN、UART、SPI、I^2C、FlexRay	CubeSat、SmallSat	The United Kingdom
AAC Clyde Space KRYTEN-M3-PLUS	SPARC V8	50 MHz	8 MB Flash +4 MB SRAM	CAN、UART、SPI	High reliability CubeSat/SmallSat tasks	The United Kingdom
AAC Clyde Space Q7S	ARM Cortex-A9	250 M Hz	1 × 512 MB and 1 × 256 MB LPDDR2 RAM chips	SpaceWire、1553B、FlexRay、PCIe、RGMII	Low to medium orbit satellites, commercial remote sensing missions	The United Kingdom
AAC Clyde Space Sirius QuadCore	LEON4	250 MHz	16 GB Flash +4 GB DDR3	PCIe、RGMII、FlexRay、CAN	LEO/Deep Space Constellations, Scientific Exploration Tasks	The United Kingdom
AAC Clyde Space Sirius-TCM LEON3FT	LEON3FT	50 M	1 GB Flash +512 MB DDR3	FlexRay、SpaceWire、CAN	Small satellite platform, high reliability mission	The United Kingdom
AAC Clyde Space Sirius-OBC-LEON3FT	LEON3FT	50 M	1 GB Flash +512 MB DDR3	FlexRay、SpaceWire、CAN	LEO/deep space satellite, autonomous operation requirements	The United Kingdom
AAC Clyde Space Sirius TCM Dev Kit	LEON3FT	--	Engineering verification phase	Engineering verification phase	R&D testing, rapid prototyping development	The United Kingdom

management to sustain deterministic operations in space environments.

The HPC unit application software integrates four core functional modules: command and telemetry management, health monitoring with operational maintenance, and application scheduling and oversight.

The command management module facilitates deterministic data exchange via RS422 interface with the high-reliability monitoring CPU, executing reception of spacecraft management computer directives and broadcast time-code synchronization signals. Telemetry management systematically aggregates operational status parameters through periodic sampling of internal system diagnostics, structures these metrics into standardized engineering datasets for transmission to the high-reliability monitoring CPU over dedicated internal buses, and further orchestrates autonomous packaging of its operational parameters into consolidated CCSDS-compliant telemetry source packets.

Health and maintenance operations implement essential system preservation capabilities, including initialization sequences, precision time protocol synchronization, cross-bus communication integrity monitoring, and on-orbit firmware reconfiguration protocols.

The application scheduling and oversight module dynamically instantiates payload applications upon ground-commanded directives by spawning child processes with unique process identifiers, continuously monitors application runtime status and memory utilization through cyclic diagnostic checks, embeds resultant telemetry into engineering status packets, and enforces strict access constraints against frequent eMMC storage operations to mitigate radiation-induced wear and single-event

TABLE 5 The actual high-performance computing test of SPHMU.

Test Category	Configuration Parameters	Result
HPC CPU (find the maximum prime number within the search range)	--threads = 1	1.71/sec
	--Cpu-max-prime = 1,000,000	
	--threads = 2	3.42/sec
	--Cpu-max-prime = 1,000,000	
	--threads = 4	3.43/sec
	--Cpu-max-prime = 1,000,000	
Thread (Concurrent thread execution, time spent on loop response semaphore)	--threads = 500	Min: 0.05 ms Avg: 48.64 ms Max: 890.93 ms
	--thread-yields = 100	
	--thread-locks = 4	
Memory (Transmitting a certain amount of data throughput in different block sizes)	--threads = 1	6166.23 MiB/sec
	--memory-block-size = 8K	
	--memory-total-size = 16G	
	--memory-oper = write	
	--threads = 2	8255.39 MiB/sec
	--memory-block-size = 8K	
	--memory-total-size = 16G	
	--memory-oper = write	
	--threads = 4	8623.00 MiB/sec
	--memory-block-size = 8K	
	--memory-total-size = 16G	
	--memory-oper = write	
	--threads = 1	11,125.03 MiB/sec
	--memory-block-size = 8K	
	--memory-total-size = 16G	
	--memory-oper = read	
	--threads = 2	21,483.41 MiB/sec
	--memory-block-size = 8K	
	--memory-total-size = 16G	
	--memory-oper = read	
	--threads = 4	21,855.56 MiB/sec
	--memory-block-size = 8K	
	--memory-total-size = 16G	
	--memory-oper = read	

functional interrupts. Figure 9 is the Linux program running interface of SPHMU.

4 Experiment of SPHMU

As a standardized aerospace device, the SPHMU has undergone comprehensive acceptance-level environmental testing including Environmental Stress Screening (ESS) thermal cycling, functional thermal cycling, mechanical assessments comprising random and sinusoidal vibration profiles, thermal vacuum validation, electromagnetic compatibility (EMC) verification, residual magnetic field measurement, and electrostatic discharge (ESD) immunity trials, demonstrating robust performance stability across all parameters, memory playback data integrity, and consistent software execution throughout the validation campaign. EMC testing equivalently complies with IEC 61000–4 compliance requirements. The thermal vacuum test standards are shown in Table 3.

During environmental testing, the operational temperature range of the SPHMU, module spans from −15 °C to +80 °C, compliant with the thermal control requirements specified for satellite systems.

During the environmental testing phase of the SPHMU, the operational execution of the High-Performance Computing (HPC) unit's software is illustrated in Figure 10, which is orbital data reception and computational processing from Channel 0 of the MIL-STD-1553B bus, demonstrating sustained deterministic functionality and fault-free performance under simulated mission profiles, with zero deviations in computational throughput, memory integrity, or task completion deadlines observed throughout thermal, mechanical, and electromagnetic stress profiles equivalent to worst-case orbital conditions. Sphmu in thermal vacuum test is shown in Figure 11.

We conducted a detailed comparison of OBC performance both domestically and internationally, and the comparison results are shown in Table 4. Based on the comparison results in the manual, we consider using LOONGSON XX2000 CPU as our HPC main chip. Because it can be seen from Table 4 that XX2000 has a higher frequency and can perform faster operations, the results of which are shown in Table 5. XX2000 also has a larger DDR4 SDRAM runtime capacity, which can handle more tasks.

5 Conclusion

This paper introduces a novel architecture for spaceborne intelligent computing and intelligent data processing, leveraging synergistic operation between a High-Reliability Computer (HRC) and a High-Performance Computer (HPC) to simultaneously achieve robust payload management with deterministic data interchange and advanced computational capabilities for on-orbit intelligence in space applications. Within this framework, the HRC exclusively manages all spacecraft bus interactions, including telecommand/telemetry operations for diverse payloads and spatiotemporal information synchronization, while the HPC executes specialized application software (Apps) for processing payload-derived datasets—particularly computation-intensive tasks such as real-time attitude determination, orbital trajectory propagation, and navigation solutions demanding significant processing throughput.

The Space Payload Health Management Unit (SPHMU) designed for specified mission profiles embodies this architecture through a highly integrated and radiation-hardened platform, integrating an HPC alongside a retained HRC to enable space-grade high-performance computing and data processing; consequently, it preserves fundamental payload management and data handling functionalities inherent in conventional units while augmenting capabilities with advanced computational modules, including real-time precision orbit determination algorithms, autonomous maneuver software for elliptical trajectories, and intelligent on-orbit analytics with anomaly detection systems—all deployable as containerized applications via dedicated hardware supporting software-defined installation paradigms.

This innovative architecture for spaceborne high-performance computing and intelligent data processing establishes a technological foundation extensible to future space stations, low-Earth-orbit observation missions, medium/high-Earth-orbit exploration platforms, and deep-space probes; furthermore, its Linux-based desktop-like operational interface significantly enhances astronaut usability during scientific operations, offering intuitive control for complex computational tasks while exhibiting exceptional adaptability across diverse space mission profiles through its open architecture and containerized software ecosystem.

Data availability statement

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

Author contributions

WZ: Project administration, Visualization, Formal Analysis, Writing – original draft, Data curation, Conceptualization, Investigation, Methodology. JR: Visualization, Data curation, Validation, Writing – review and editing, Conceptualization. MM: Software, Writing – original draft. JZ: Supervision, Methodology, Writing – review and editing. SL: Supervision, Writing – original draft. WJ: Writing – original draft, Validation. ZD: Investigation, Conceptualization, Writing – original draft. BH: Investigation, Writing – original draft, Methodology, Data curation. GX: Investigation, Writing – review and editing, Conceptualization, Formal Analysis, Project administration. GY: Supervision, Visualization, Writing – original draft. YZ: Investigation, Writing – review and editing. JA: Conceptualization, Investigation, Writing – review and editing.

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Conflict of interest

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